

OSLO2

CPU : Intel Penryn-6M (1067/800) MHz
 Chip Set : Intel Cantiga & ICH9M
 Remarks : Montevina Platform

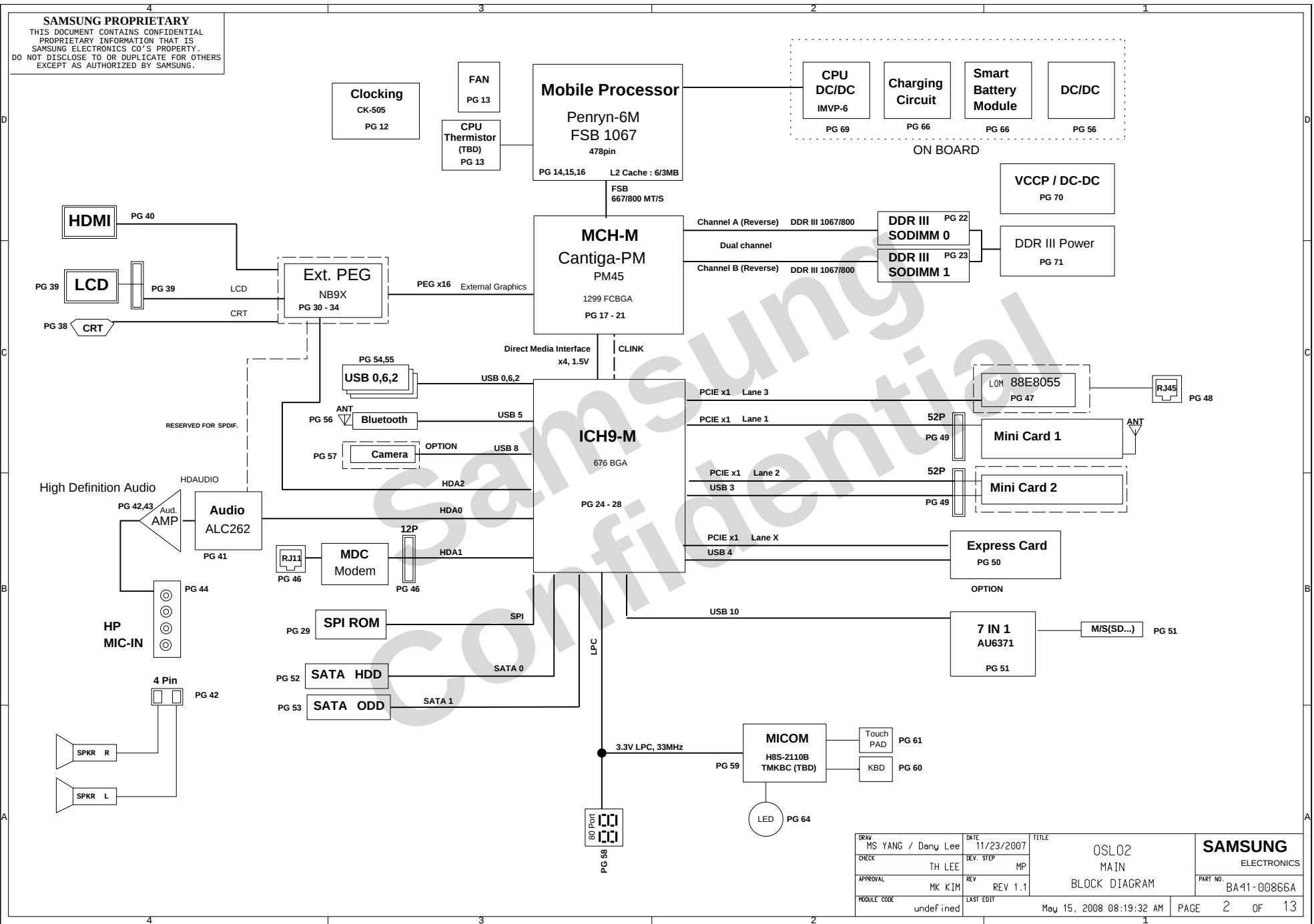
Model Name : Oslo2_DDR3
 PBA Name : MAIN
 PCB Code : BA41-00866A
 BA41-00867A
 Dev. Step : MP
 Revision : 1.1
 T.R. Date : 2008. 05.15

DRAW	CHECK	APPROVAL
MS YANG TH LEE	TH LEE	MK KIM

■ Owner : SEC Mobile R & D Signature : X

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CHECK	TH LEE	DEV. STEP	MP		MAIN	
APPROVAL	MK KIM	REV	REV 1.1		COVER	
MODULE CODE		LAST EDIT	May 15, 2008 08:19:32 AM	PAGE	1	PART NO. BA41-00866A
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DRAW MS YANG / Dany Lee	DATE 11/23/2007	TITLE OSL02 MAIN BLOCK DIAGRAM	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK TH LEE	DEV. STEP MP		
APPROVAL MK KIM	REV REV 1.1		
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BOARD INFORMATION**SCHEMATIC ANNOTATIONS AND BOARD INFORMATION****PCI Devices**

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	A,B,C
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
GLAN	-	-	F

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH9-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	Marvell LAN (88E8850)
Crystal	12MHz	Multi Card Reader	Alkor AU6371

LCD Pannel Detect (EDID)

Devices	Resolution	PANNEL_DETECT_0
---------	------------	-----------------

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core Voltage for CPU
GFX_CORE	Core Voltage for GPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH9-M
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail for DDR (off in S4-S5)
P0.75V	0.75V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_ALW	5.0V always power rail

I²C / SMB Address

Devices	Address	Hex	Bus
ICH9-m	Master	-	SMBUS Master
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
MICOM	Master	-	SMBUS Master
Battery	0001011x	16h	Battery
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor (EMC2012)

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 2
1	NC
2	SYSTEM PORT 1
3	Mini Card
4	Express Card
5	Bluetooth
6	SYSTEM PORT 2
7	NC
8	Camera
9	NC
10	Multi Card Reader (7-in-1)
11	NC

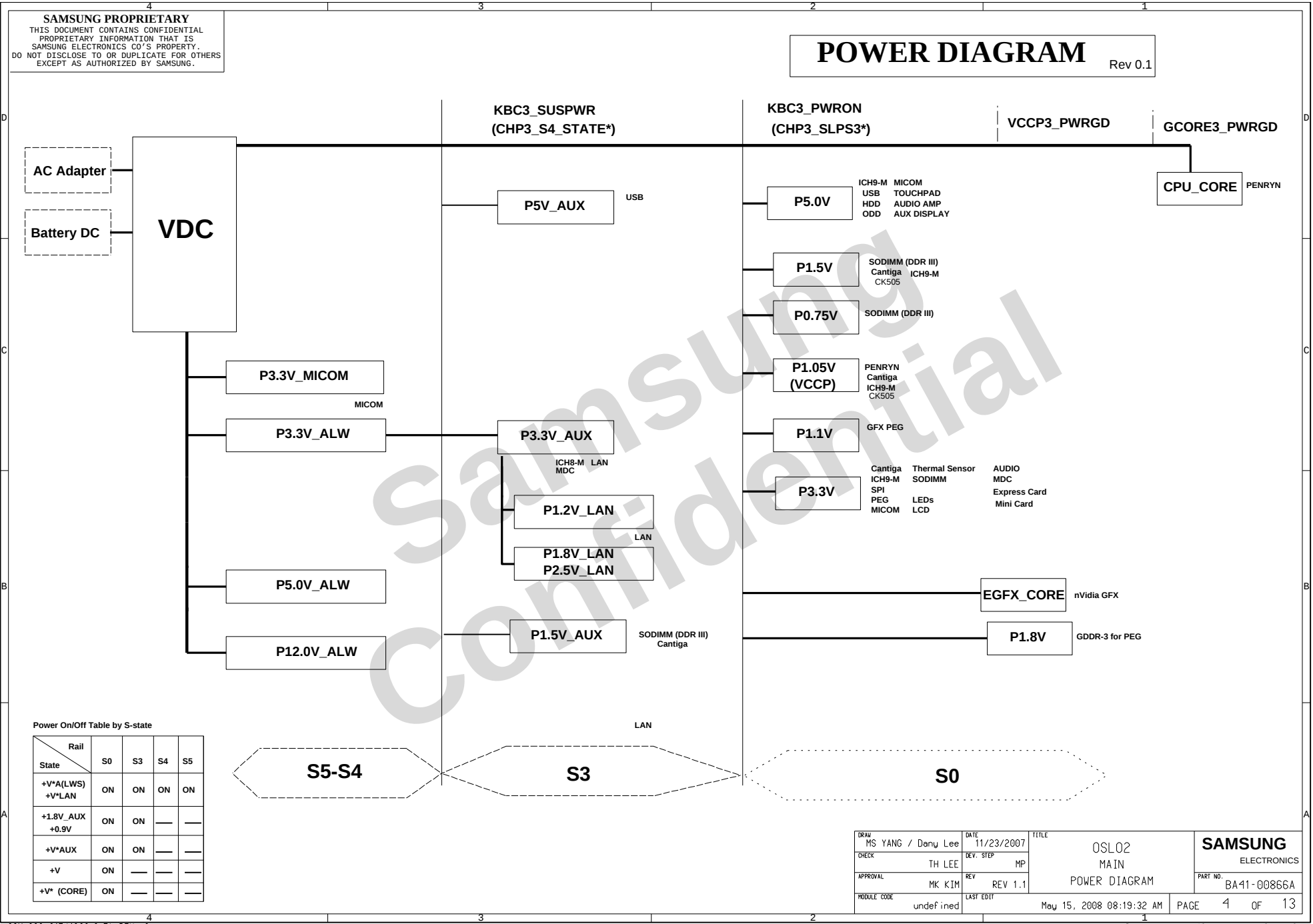
PCI Express Assign

PORT #	ASSIGNED TO
1	Mini Card 1 (WLAN)
2	Mini Card 2 (ROBSON or DVB-T)
3	Express Card
4	LOM
5	NC
6	NC

REVISION HISTORY

See rev notes for more information.

DRAW MS YANG / Dany Lee	DATE 11/23/2007	TITLE OSLO2 MAIN BOARD INFO	SAMSUNG ELECTRONICS
CHECK TH LEE	DEV. STEP MP		PART NO. BA11-00866A
APPROVAL MK KIM	REV REV 1.1		
MODULE CODE undefined	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE 3 OF 13



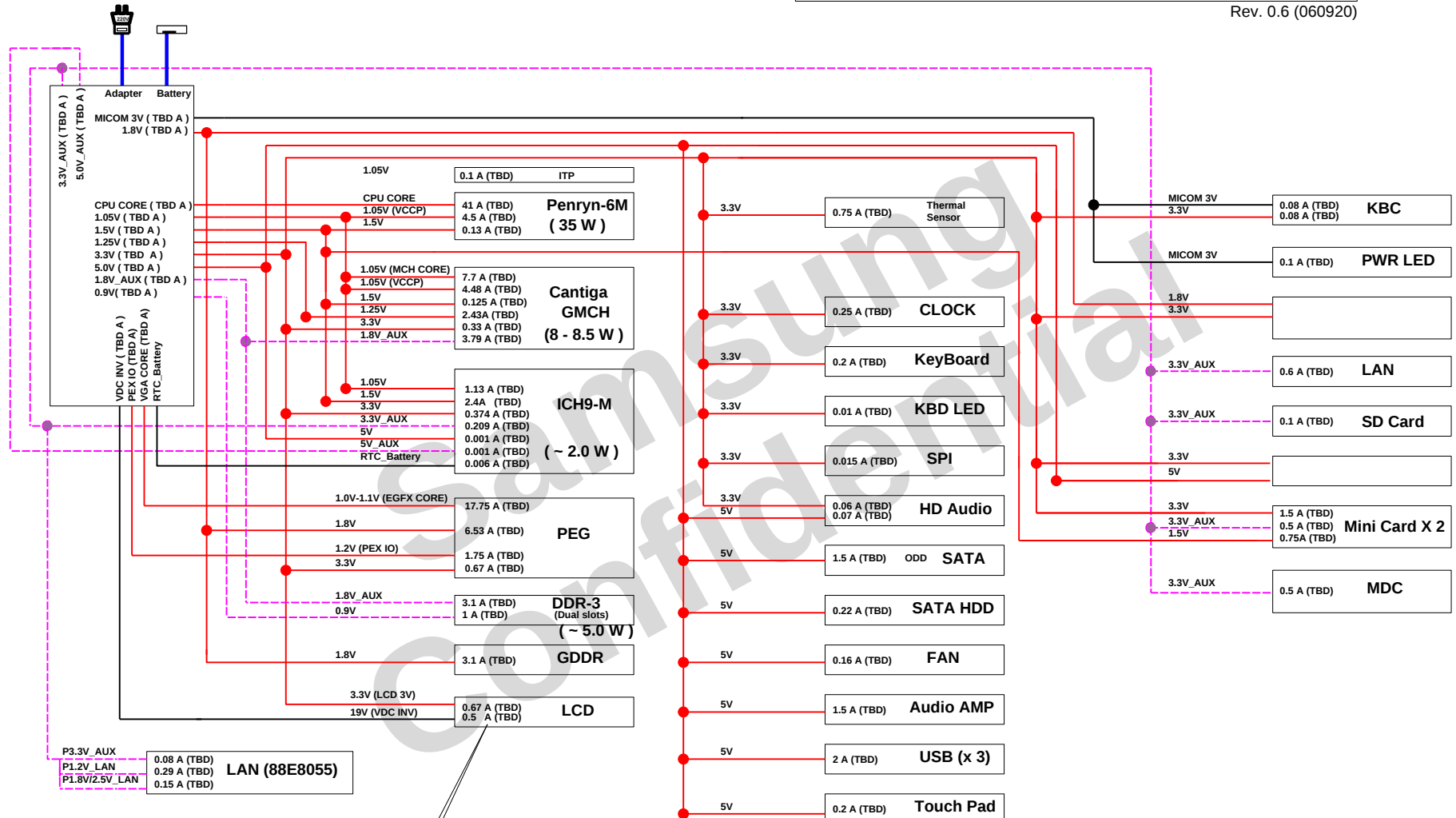
COM-22C-015(1996.6.5) REV. 3

D:/users/mobile16/mentor/oslo2/oslo2.pr

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POWER RAILS ANALYSIS

Rev. 0.6 (060920)

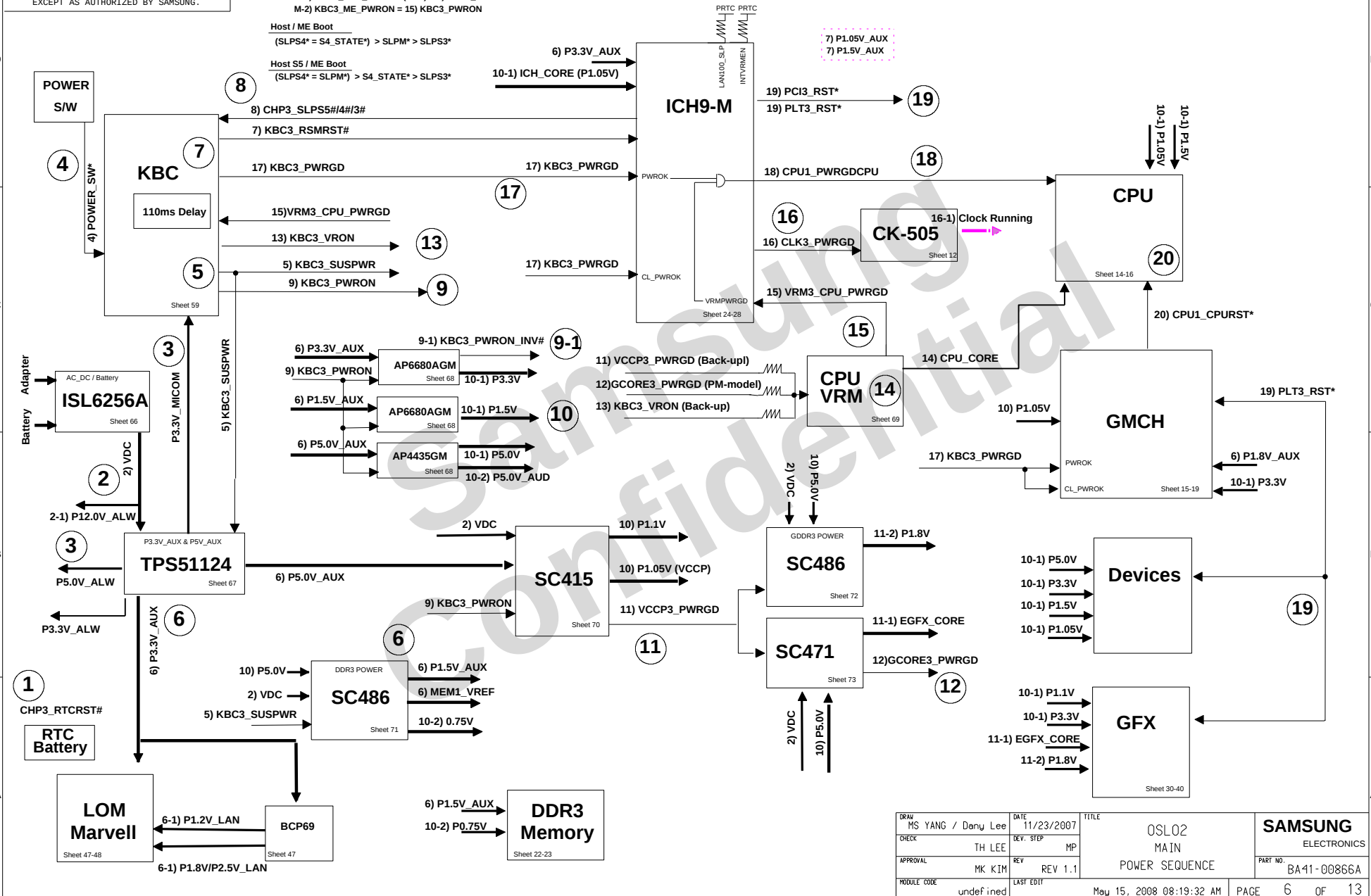


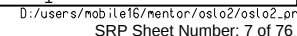
Value by Datasheet/Application notes (Value by measurement)

DRAW	MS YANG / Dany Lee	DATE	11/23/2007	TITLE	OSLO2 MAIN POWER RAILS	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP			PART NO. BA41-00866A
APPROVAL	MK KIM	REV	REV 1.1			
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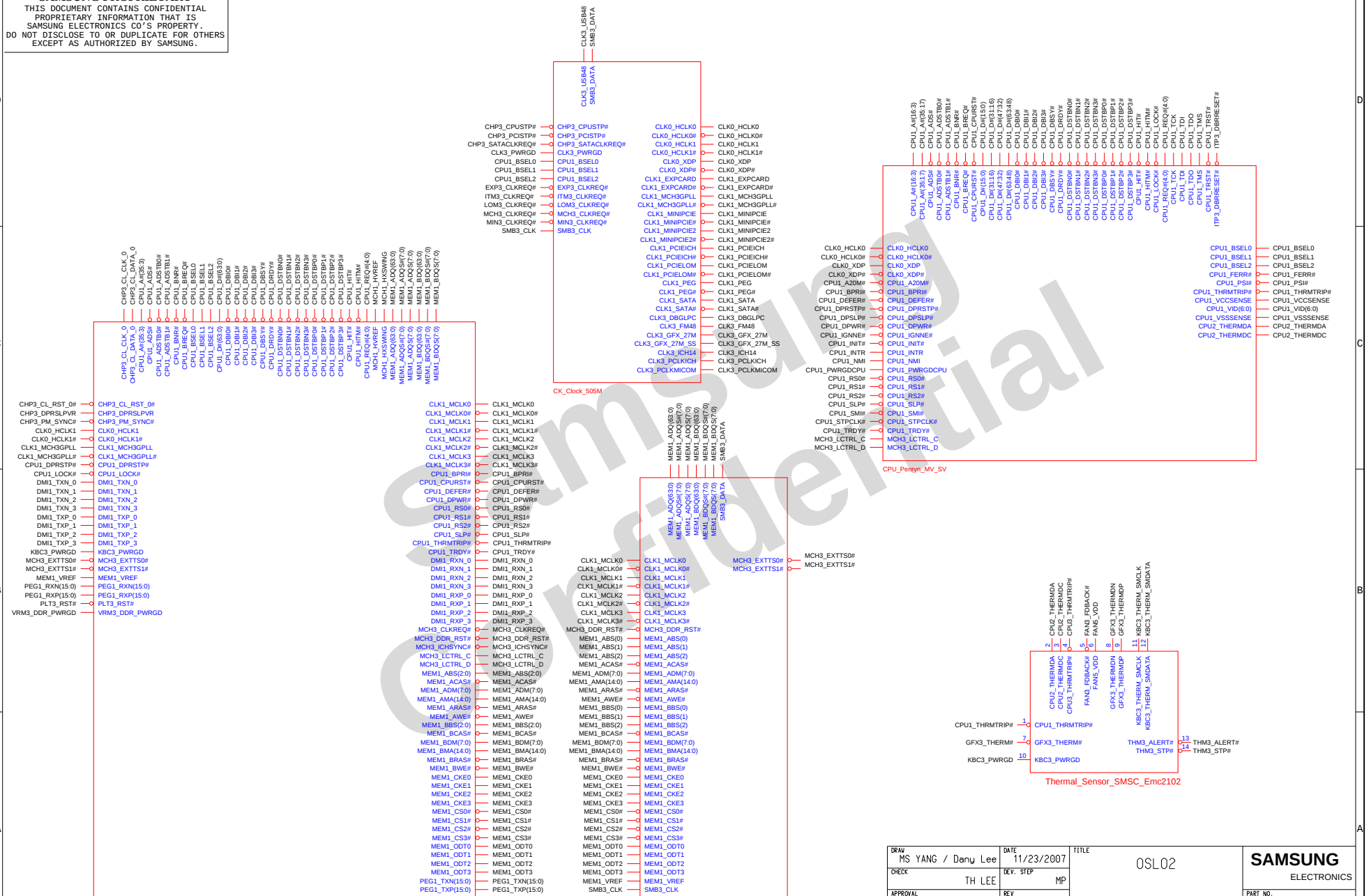
POWER SEQUENCE

Rev. 0.9





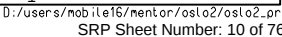
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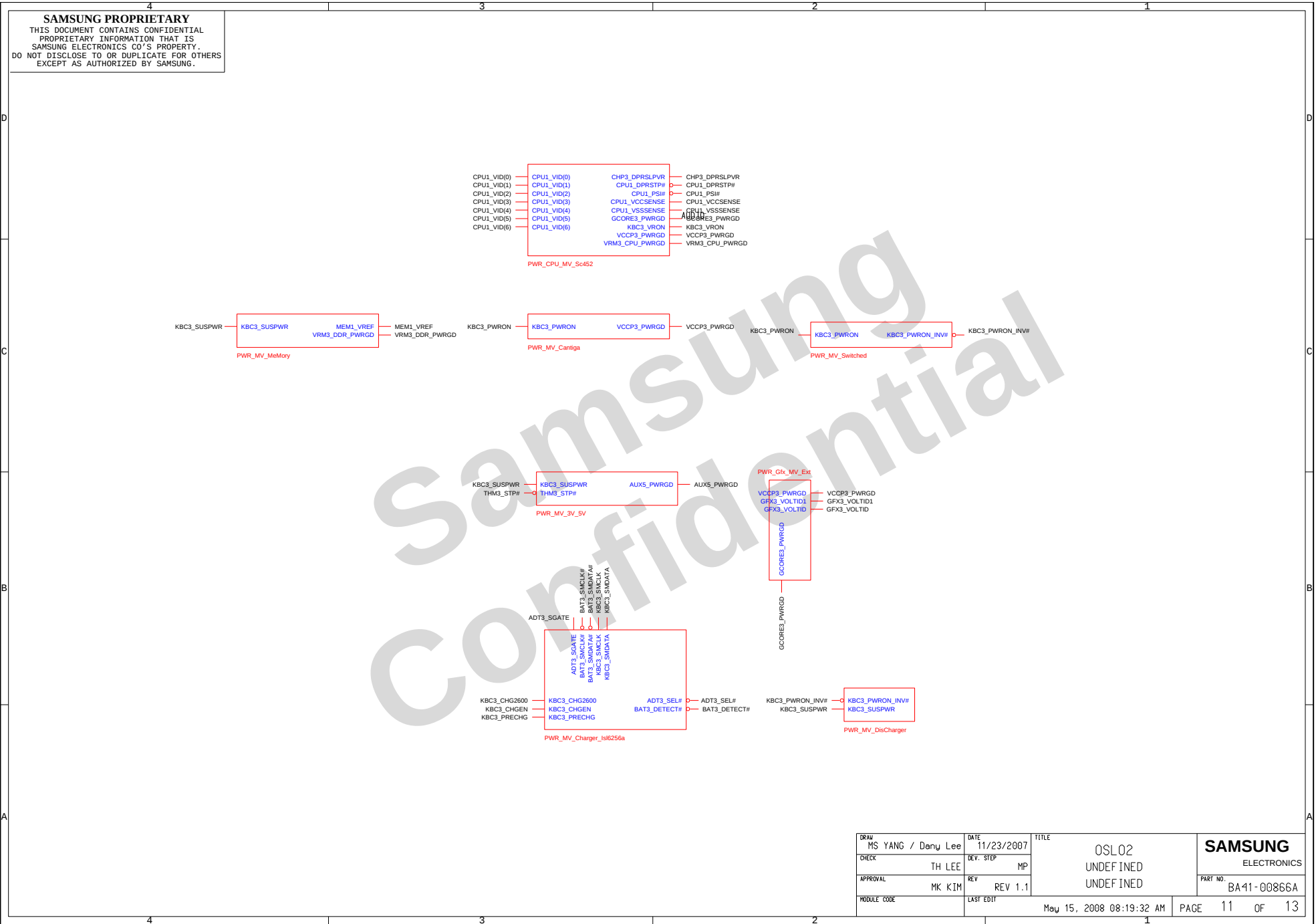


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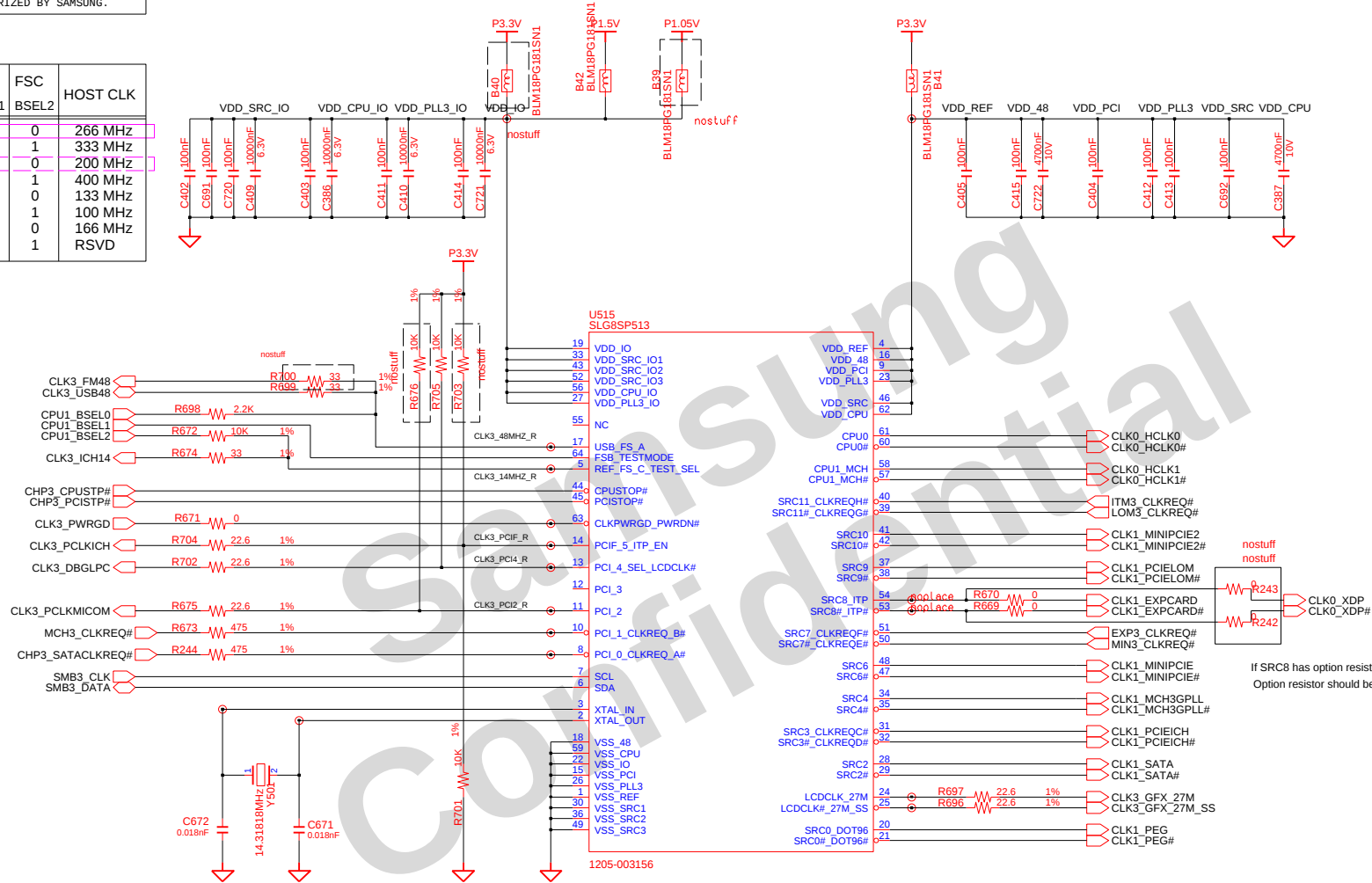




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FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATACLKREQ#	SRC2
CLK REQ B	MCH3_CLKREQ#	SRC4
CLK REQ E	MIN3_CLKREQ#	SRC6
CLK REQ F	EXP3_CLKREQ#	SRC8
CLK REQ G	LOM3_CLKREQ#	SRC9

SEL_LCDCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	PEG_CLK/PEG_CLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

Place 14.318MHz within
 500mils of CK-505

2nd source IDT, 1205-003159

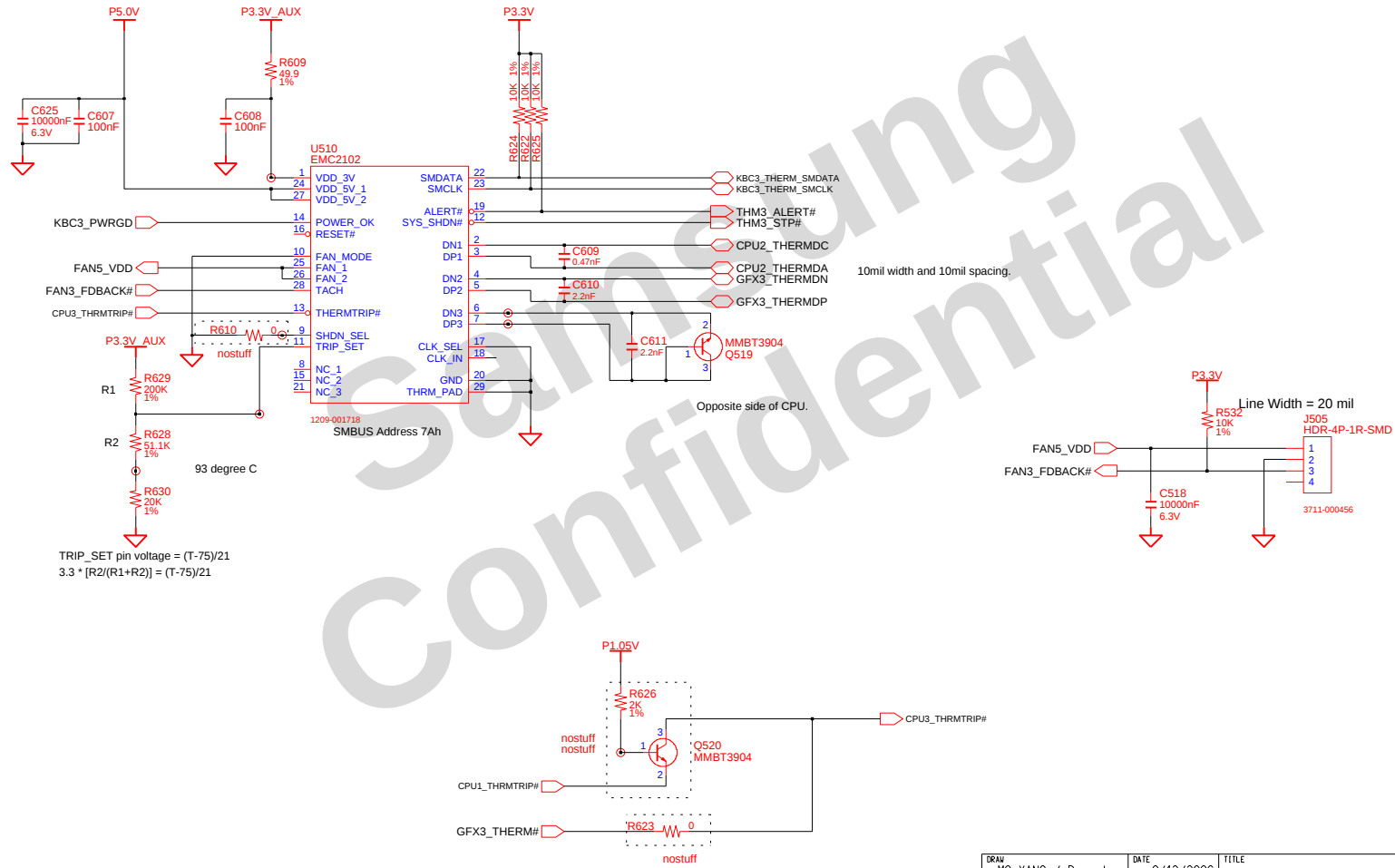
This part is 64pin QFN package.

DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02 Main_Clock_Circuit CK-Clock_505M	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK TH LEE	DEV. STEP MP	REV 1.1	
APPROVAL MK KIM	REV 1.1	LAST EDIT May 15, 2008 08:19:32 AM	PAGE 1 OF 1
MODULE CODE undefined			

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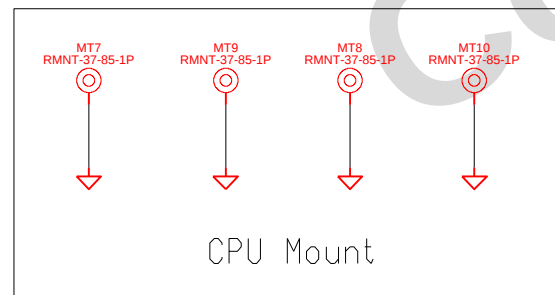
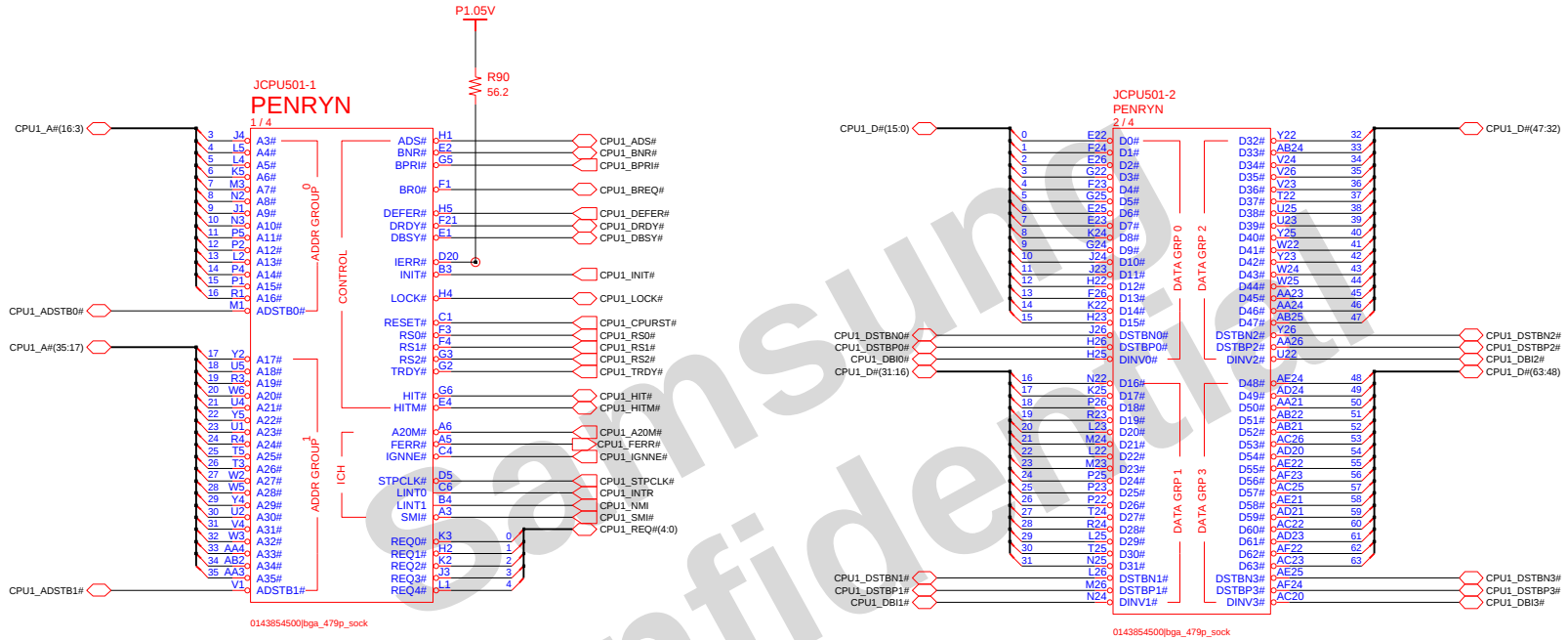
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THERMAL SENSOR & FAN CONTROL



DRAW	MS YANG / Dany Lee	DATE	8/12/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP	thermal_Sensor_SMSC_Emc2102	PART NO.	
APPROVAL	MK KIM	REV	REV 1.1	thermal_Sensor_SMSC_Emc2102	BA41-00866A	
MODULE CODE		LAST EDIT		May 15, 2008 08:19:32 AM	PAGE 1 OF 1	

479P CPU socket is 3704-001153



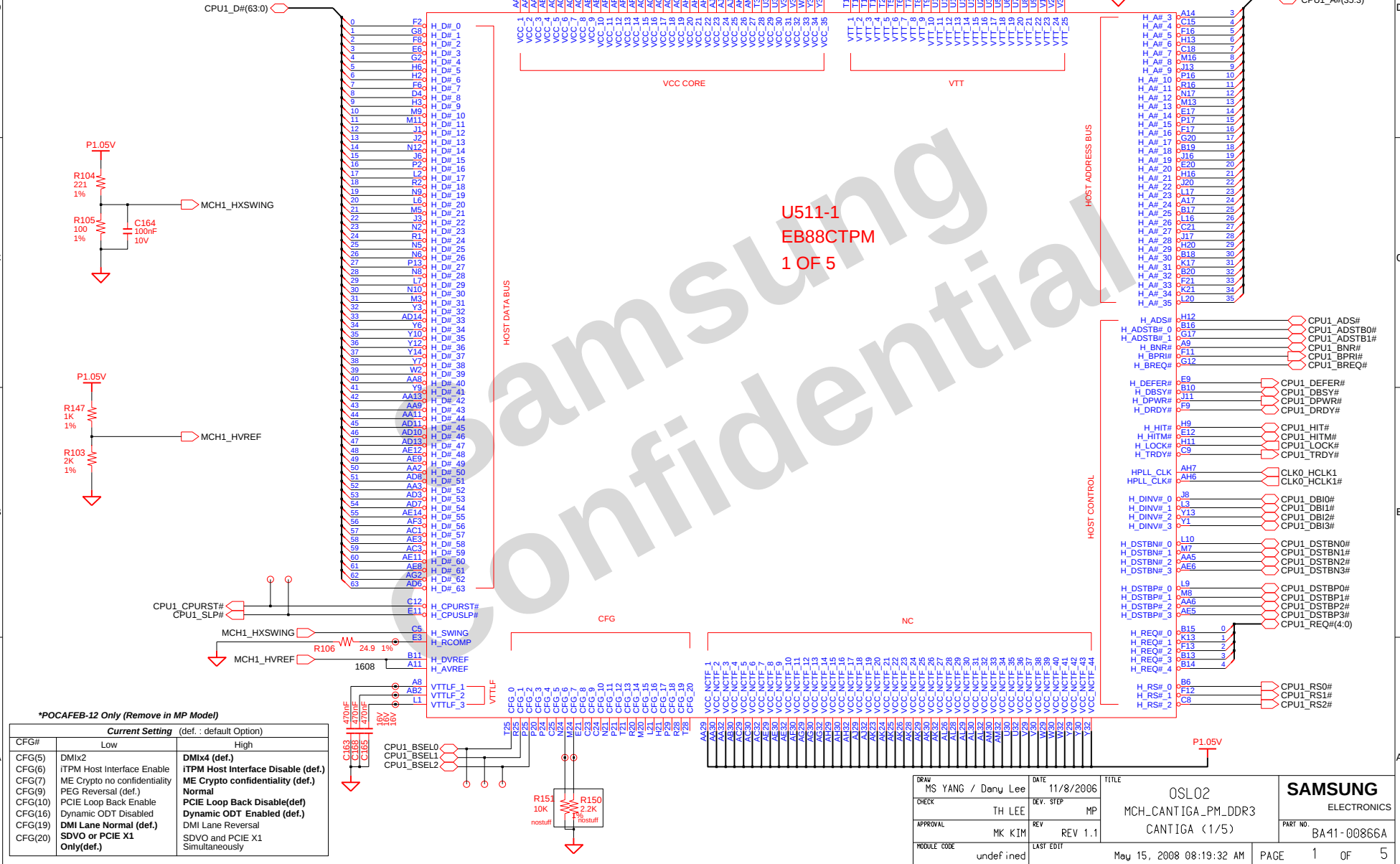
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CHECK TH LEE	DEV. STEP MP		PART NO. BA11-00866A
APPROVAL MK KIM	REV REV 1.1		
MODULE CODE undefined	LAST EDIT May 15, 2008 08:19:32 AM	PAGE 1 OF 3	

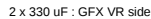
JCPU501-3
PENRYN
3 / 4



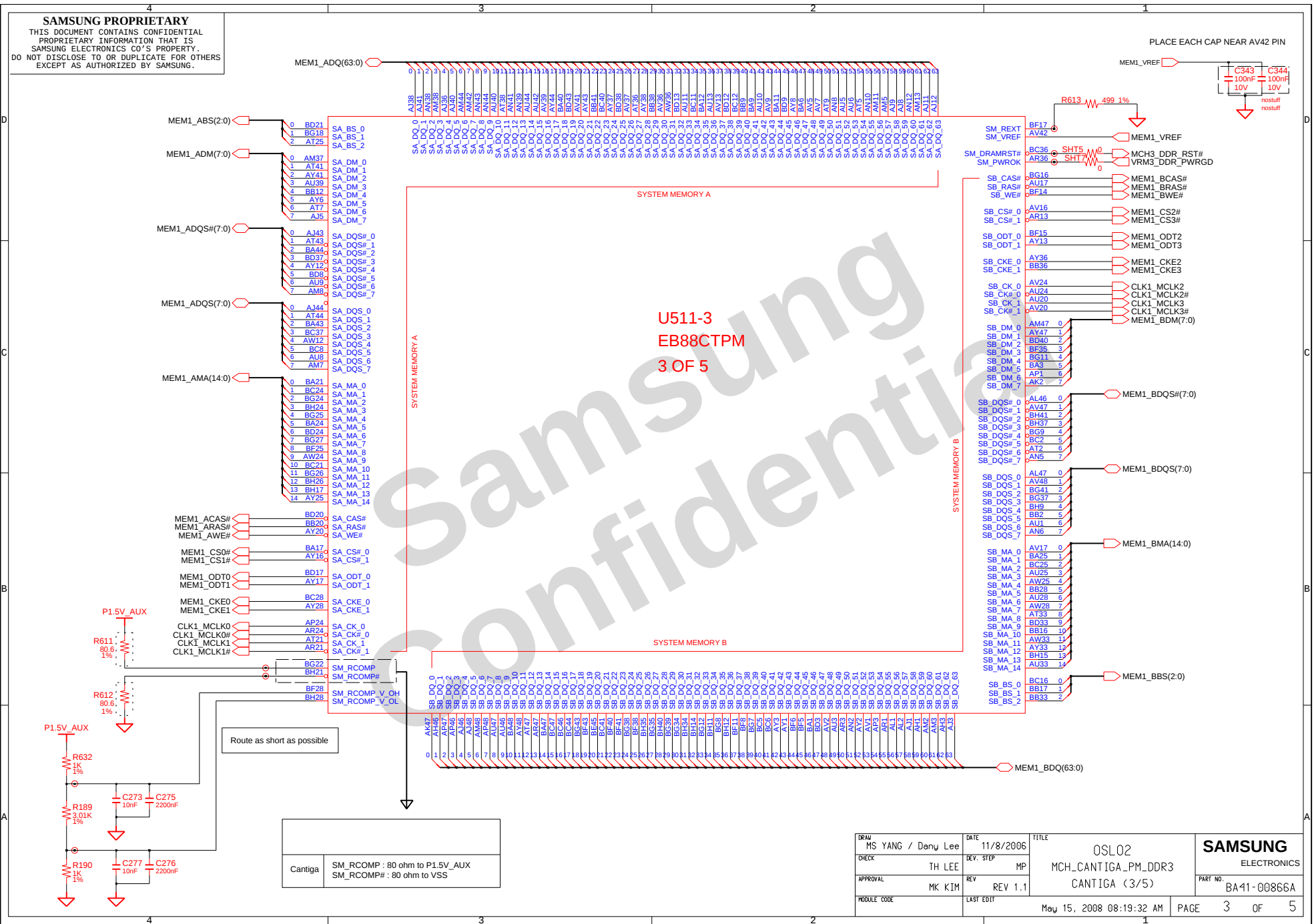
	Pull-up	Pull-down
FSB 1067 MHz FSB 800 MHz	BSEL1	BSEL0, BSEL1, BSEL2 BSEL0, BSEL2

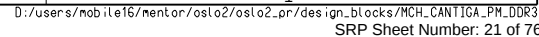
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D:/users/mobile16/mentor/oslo2/oslo2_pr/design_blocks/MCH_CANTIGA_PM_DDR3



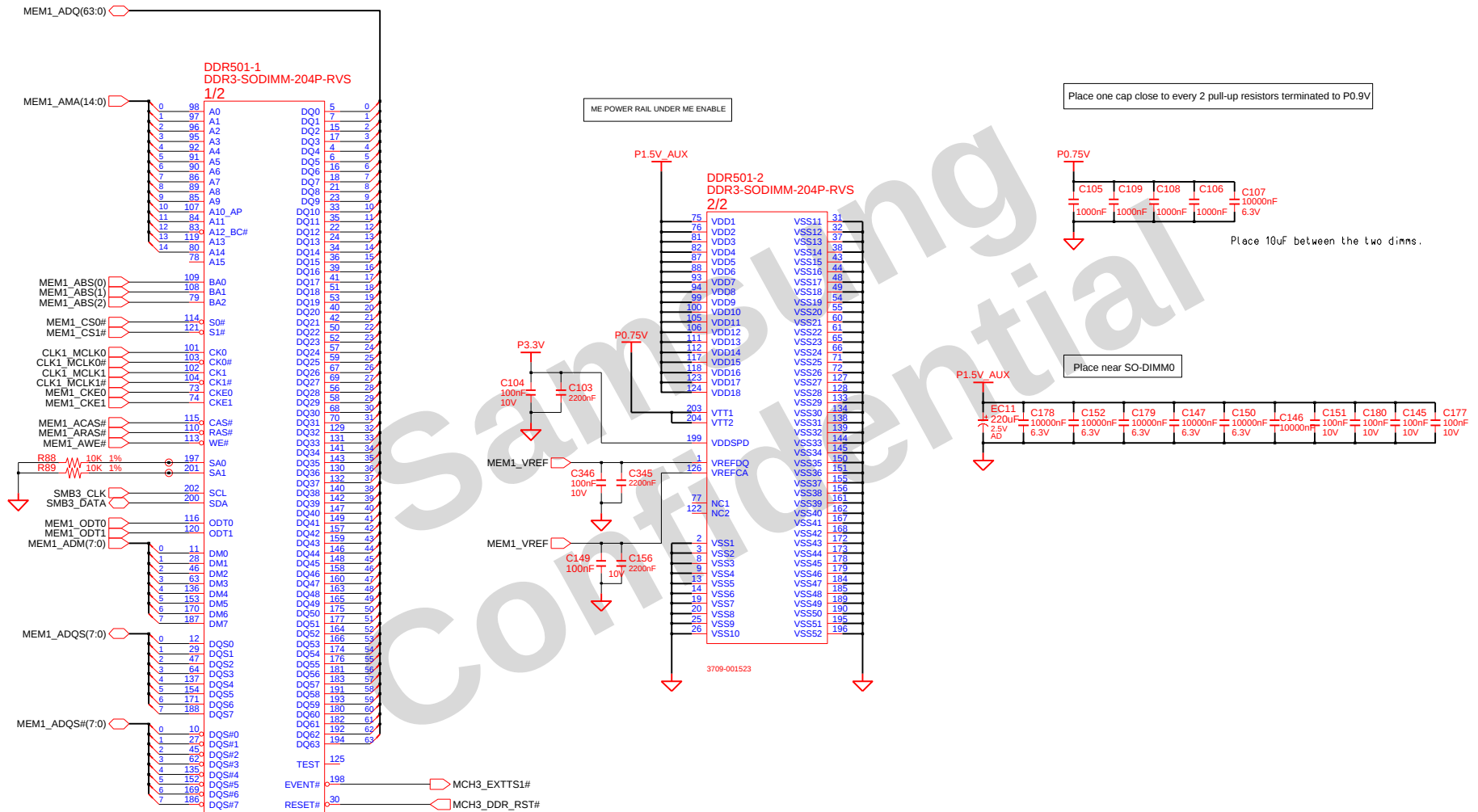


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PART NO. BA41-00866A

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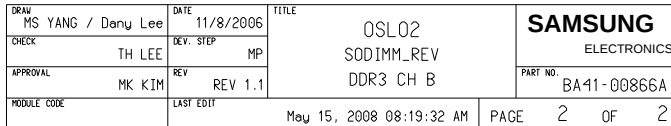
DDR SO-DIMM #0

Height : 5.2mm (Reverse)



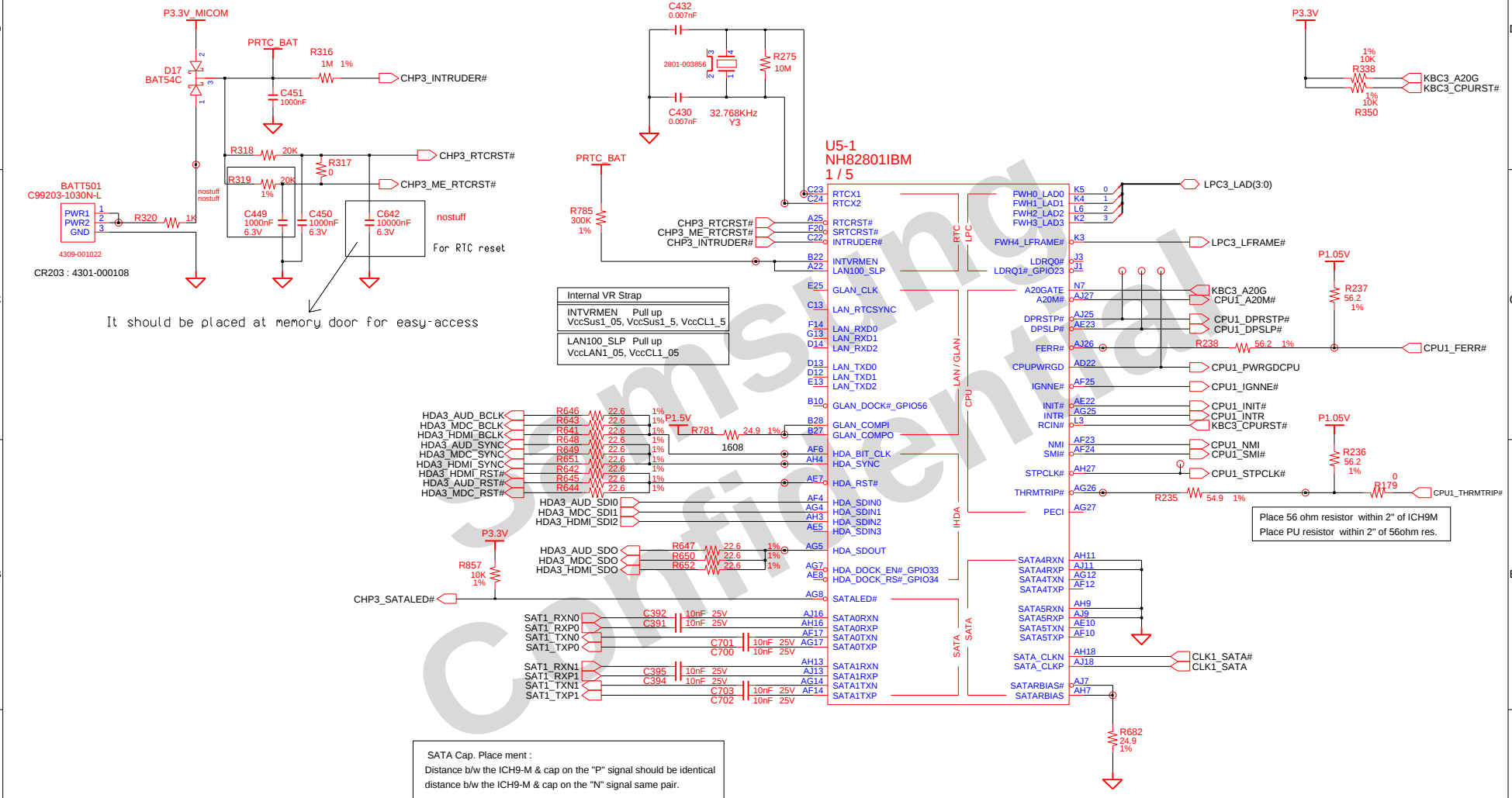
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CHECK TH LEE	DEV. STEP MP		
APPROVAL MK KIM	REV REV 1.1		
MODULE CODE	LAST EDIT		
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DDR SO-DIMM #1
Height : 9.2mm (Reverse)



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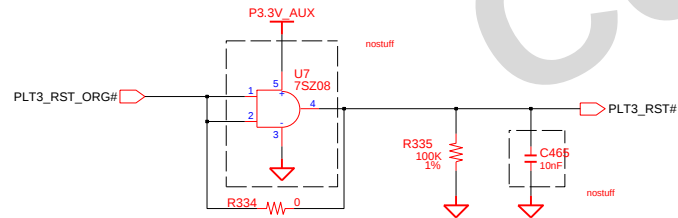
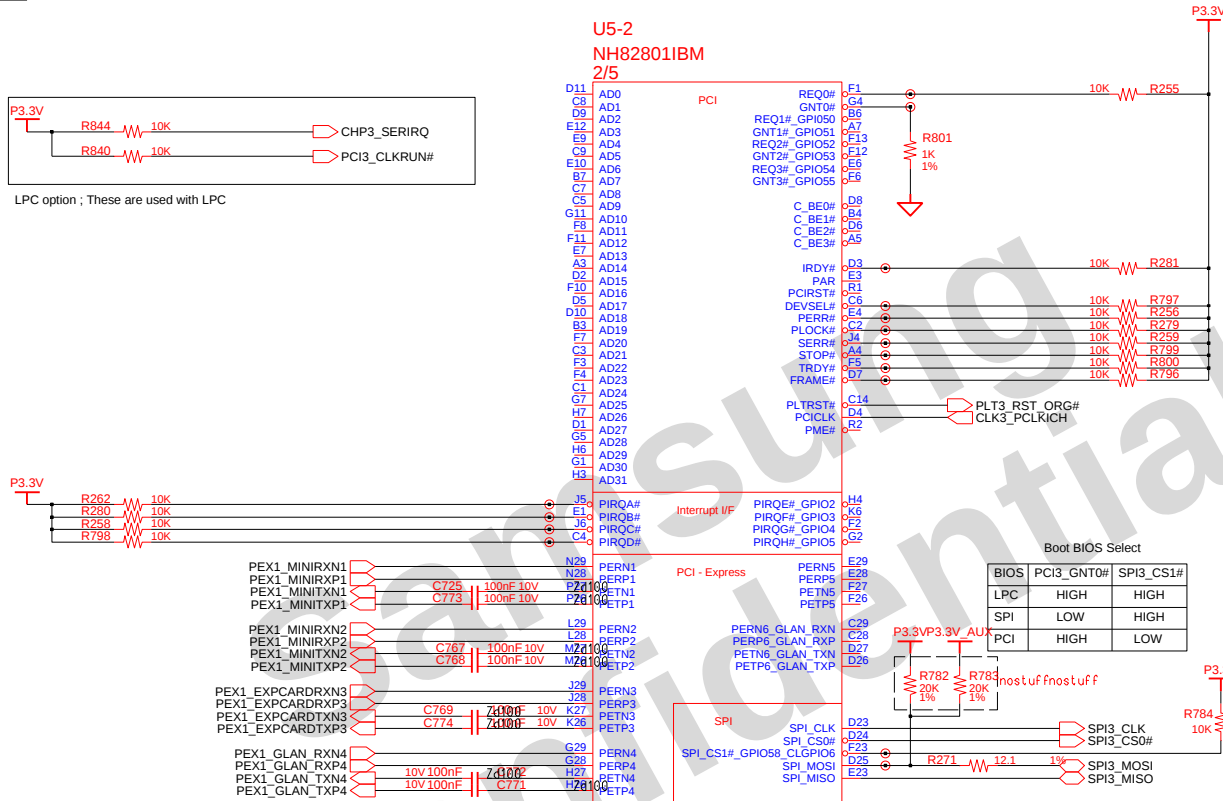


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APPROVAL	MK KIM	REV	1.1		ICH9-M (1/5)	PART NO. BA11-00866A
MODULE CODE		LAST EDIT				

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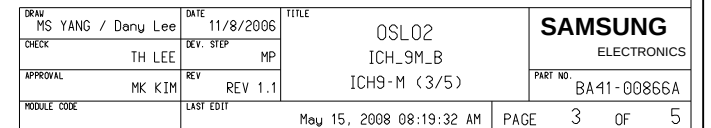
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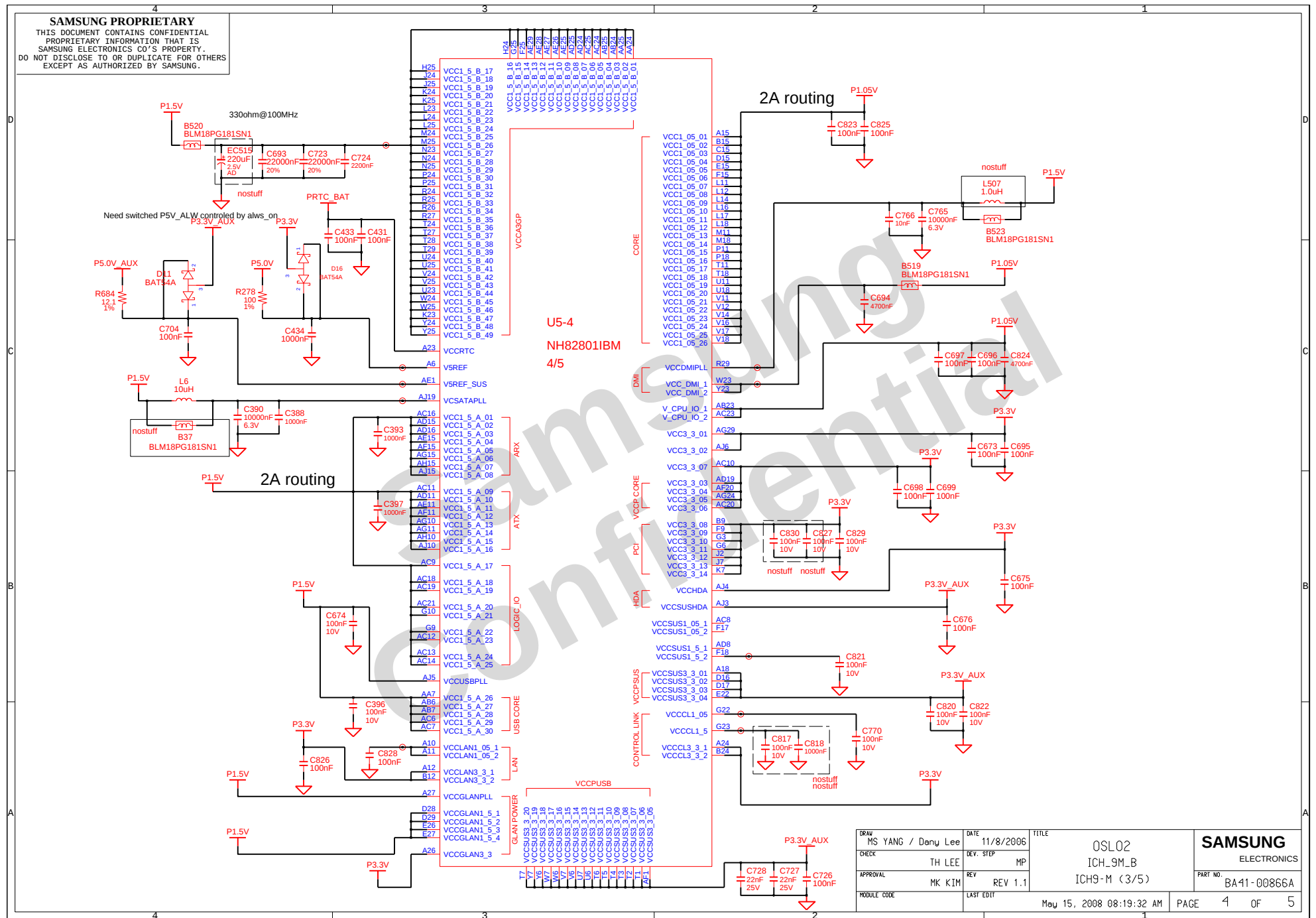


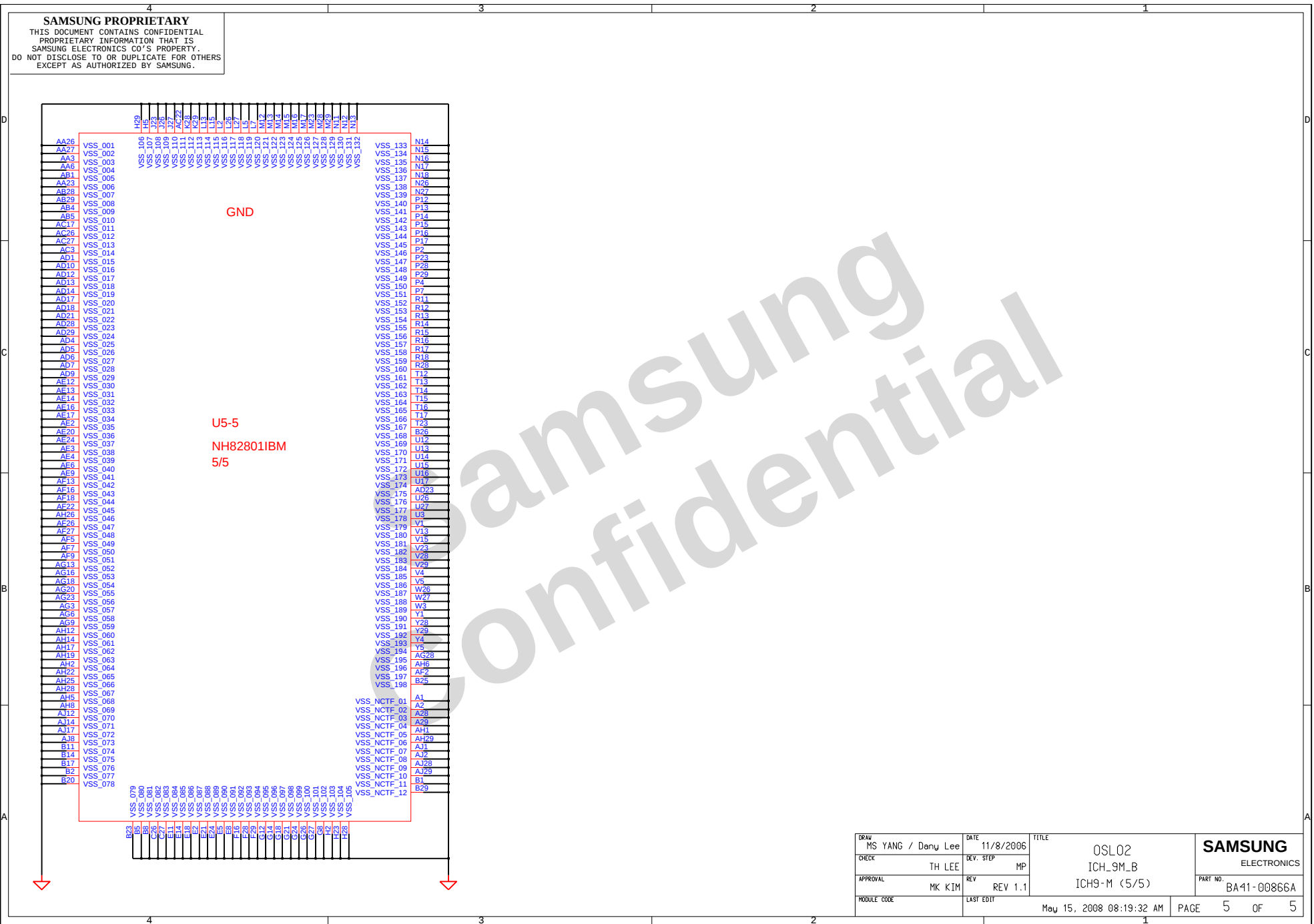
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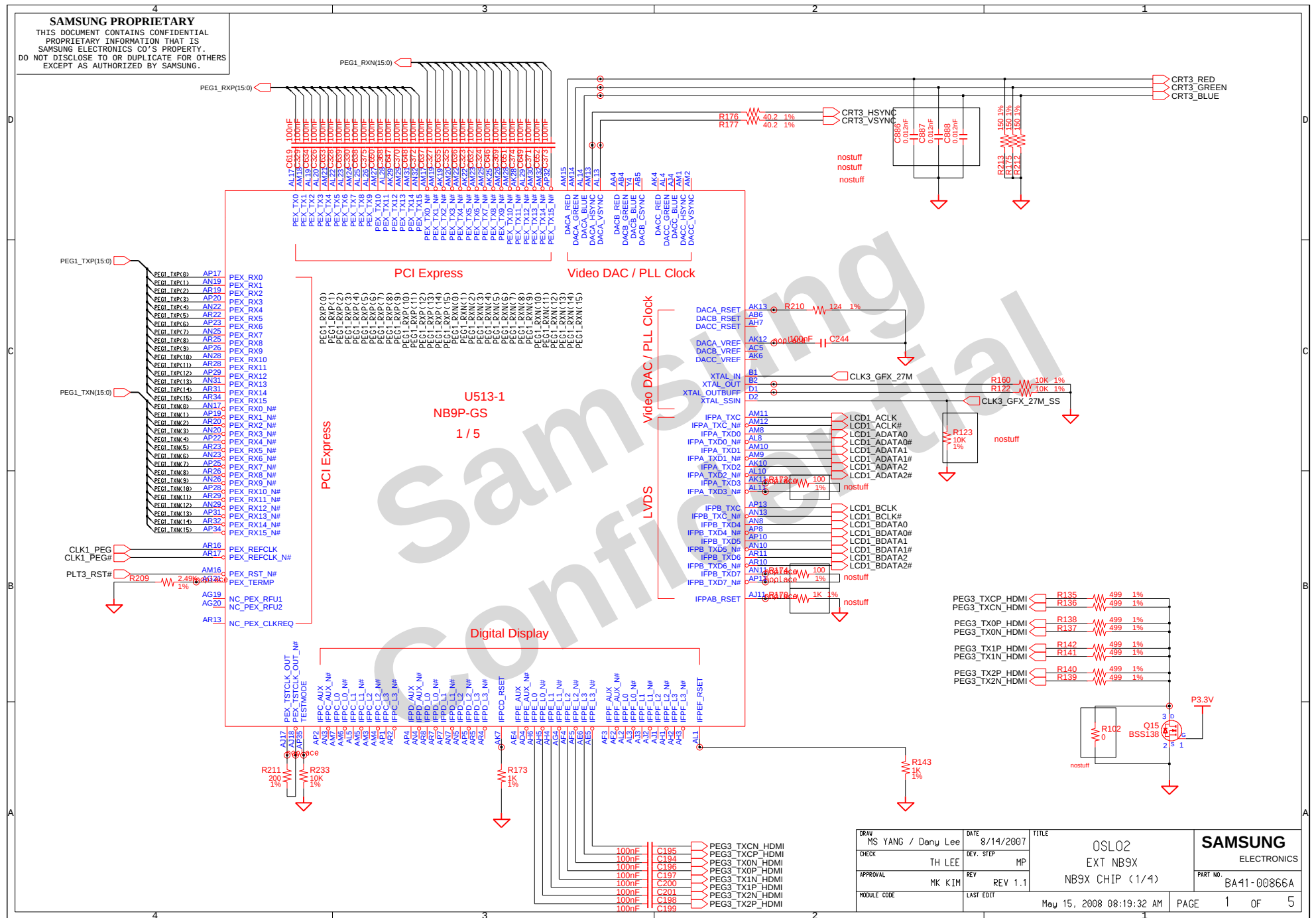
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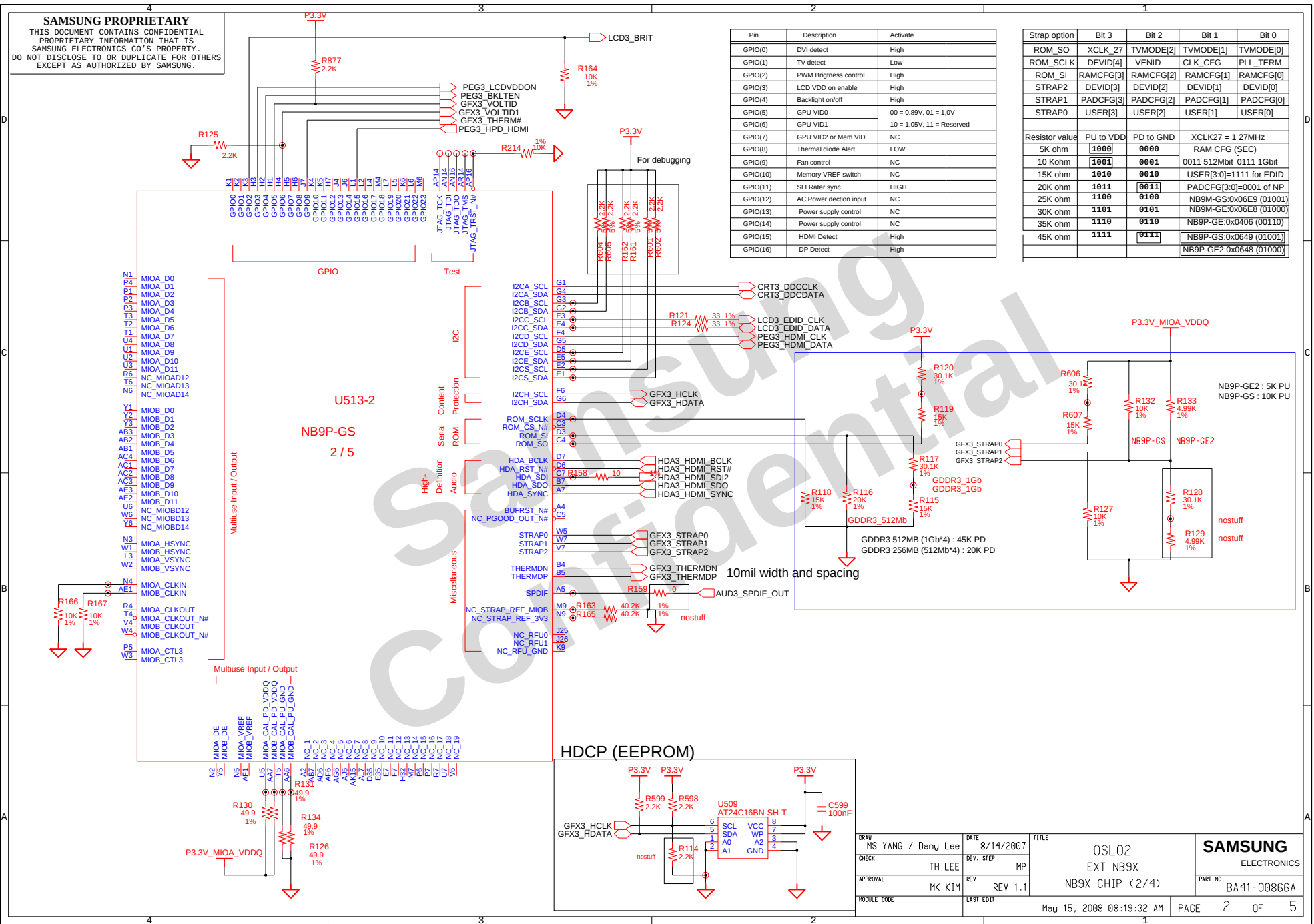




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SRP Sheet Number: 29 of 76





Pin	Description	Activate
GPIO(0)	DVI detect	High
GPIO(1)	TV detect	Low
GPIO(2)	PWM Brightness control	High
GPIO(3)	LCD VDD on enable	High
GPIO(4)	Backlight on/off	High
GPIO(5)	GPU VDD	00 = 0.89V, 01 = 1.0V
GPIO(6)	GPU VID1	NC = 1.05V, 11 = Reserved
GPIO(7)	GPU VID2 or Mem VID	NC
GPIO(8)	Thermal diode Alert	LOW
GPIO(9)	Fan control	NC
GPIO(10)	Memory VREF switch	NC
GPIO(11)	SU Rater sync	HIGH
GPIO(12)	AC Power dection input	NC
GPIO(13)	Power supply control	NC
GPIO(14)	Power supply control	NC
GPIO(15)	HDMI Detect	High
GPIO(16)	DP Detect	High

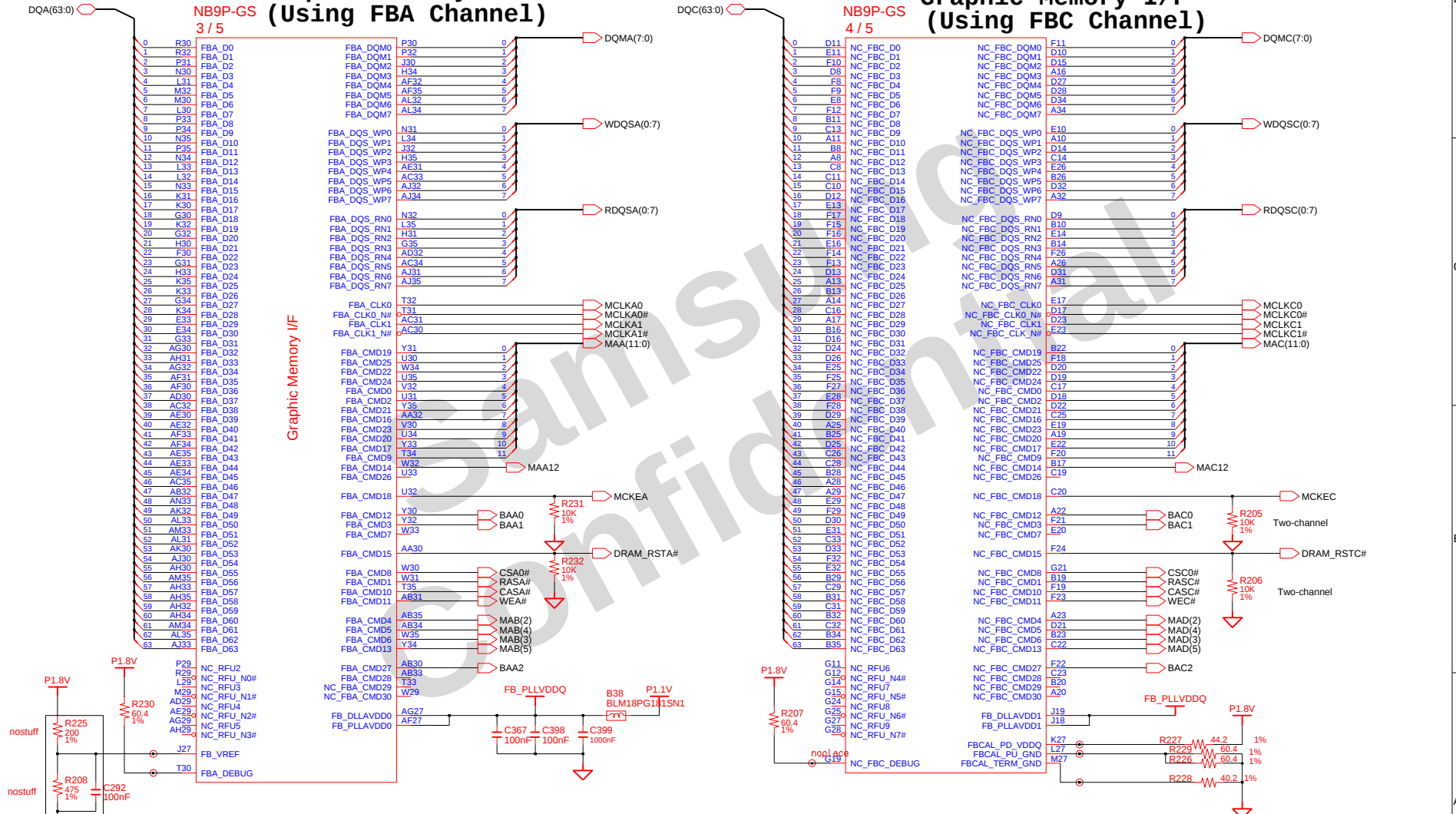
Strap option	Bit 3	Bit 2	Bit 1	Bit 0
ROM_SO	XCLK_27	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	DEVID[4]	VENID	CLK_CFG	PLL_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	DEVID[3]	DEVID[2]	DEVID[1]	DEVID[0]
STRAP1	PADCFG[3]	PADCFG[2]	PADCFG[1]	PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]

Resistor value	PU to VDD	PD to GND	XCLK27 = 1.27MHz
5K ohm	1000	0000	RAM CFG (SEC)
10 Kohm	1001	0001	0011 512Mbit 0111 1Gbit
15K ohm	1010	0010	USER[3:0]=1111 for EDID
20K ohm	1011	0011	PADCFG[3:0]=0001 of NP
25K ohm	1100	0100	NB9M-GS:0x06E9 (01001)
30K ohm	1101	0101	NB9M-GS:0x06E8 (01000)
35K ohm	1110	0110	NB9P-GS:0x0406 (00110)
45K ohm	1111	0111	NB9P-GS:0x0649 (01001)
			NB9P-GS:0x0648 (01000)

U513-3 Graphic Memory I/F
NB9P-GS (Using FBA Channel)
3/5

U513-4 Graphic Memory I/F
NB9P-GS (Using FBC Channel)
4/5

Graphic Memory I/F

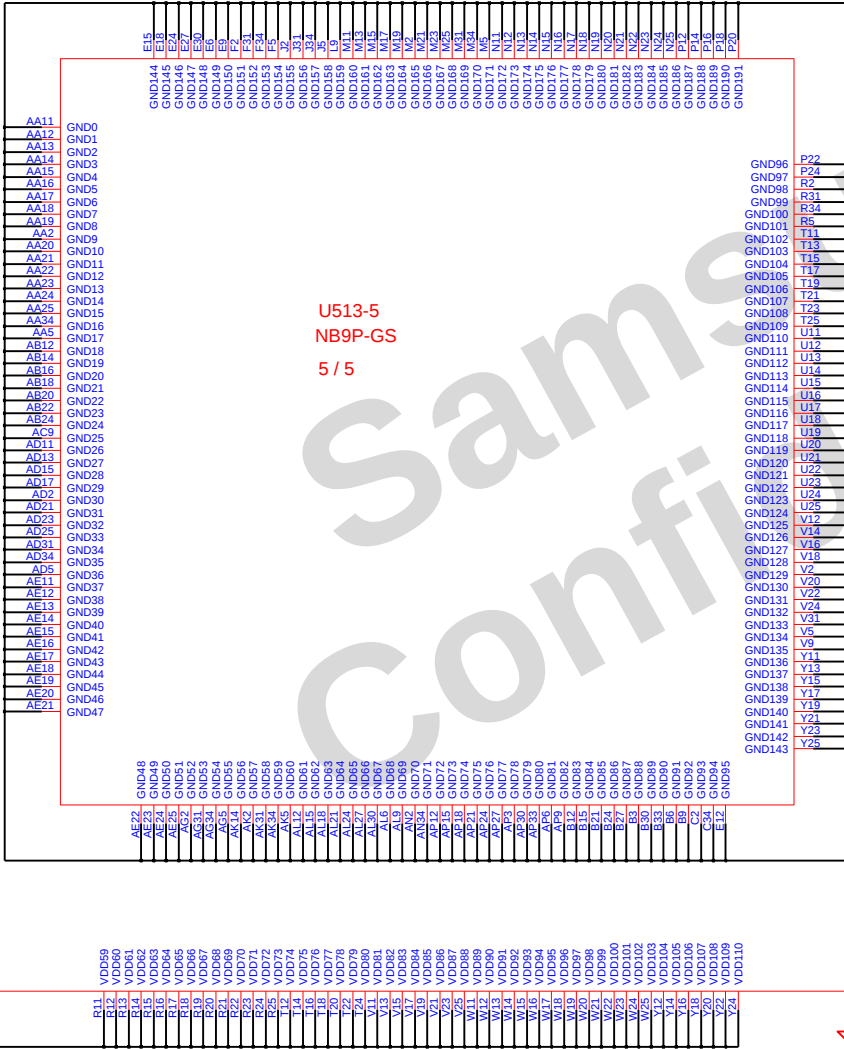


DRAW MS YANG / Dany Lee		DATE 8/14/2007	TITLE OSL02 EXT NB9X NB9X CHIP (3/4)		SAMSUNG ELECTRONICS PART NO. BA41-00866A
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APPROVAL MK KIM		REV REV 1.1			
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EGFX_CORE

AB11 VDD0
AB13 VDD1
AB15 VDD2
AB17 VDD3
AB19 VDD4
AB21 VDD5
AB23 VDD6
AB25 VDD7
AC11 VDD8
AC12 VDD9
AC13 VDD10
AC14 VDD11
AC15 VDD12
AC16 VDD13
AC17 VDD14
AC18 VDD15
AC19 VDD16
AC20 VDD17
AC21 VDD18
AC22 VDD19
AC23 VDD20
AC24 VDD21
AC25 VDD22
AD12 VDD23
AD14 VDD24
AD16 VDD25
AD18 VDD26
AD22 VDD27
AD24 VDD28
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L12 VDD30
L13 VDD31
L14 VDD32
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L16 VDD34
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M16 VDD46
M18 VDD47
M20 VDD48
M22 VDD49
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P15 VDD53
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P21 VDD56
P23 VDD57
P25 VDD58



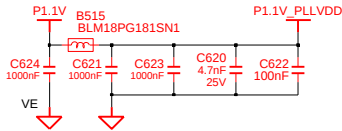
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MIOA_VDDQ1
MIOA_VDDQ2
MIOA_VDDQ3
MIOB_VDDQ0
MIOB_VDDQ1
MIOB_VDDQ2
MIOB_VDDQ3
IFPAB_PLLVDD
IFPCD_PLLVDD
IFPEF_PLLVDD

DRAW	MS YANG / Dany Lee	DATE	8/14/2007	TITLE	OSL02 EXT NB9X NB9X CHIP (4/4)	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK	TH LEE	REV. STEP	MP			
APPROVAL	MK KIM	REV	REV 1.1			
MODULE CODE		LAST EDIT				
May 15, 2008 08:19:32 AM						PAGE 4 OF 5

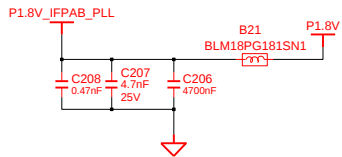
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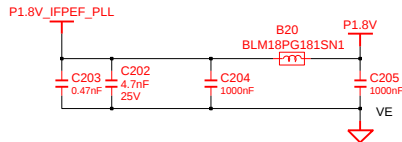
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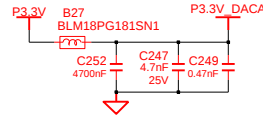
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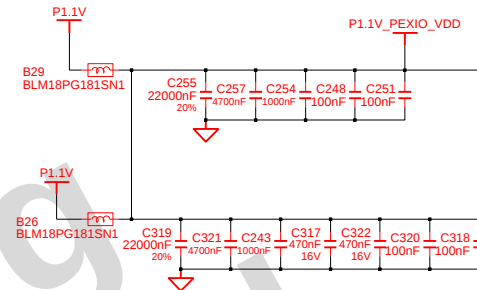
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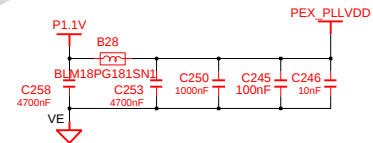
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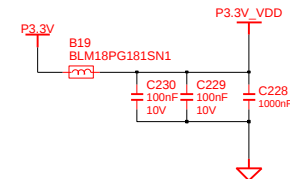
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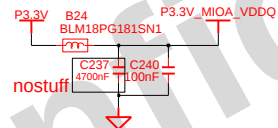
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3.3V_VDD



MIOA/B_VDDQ

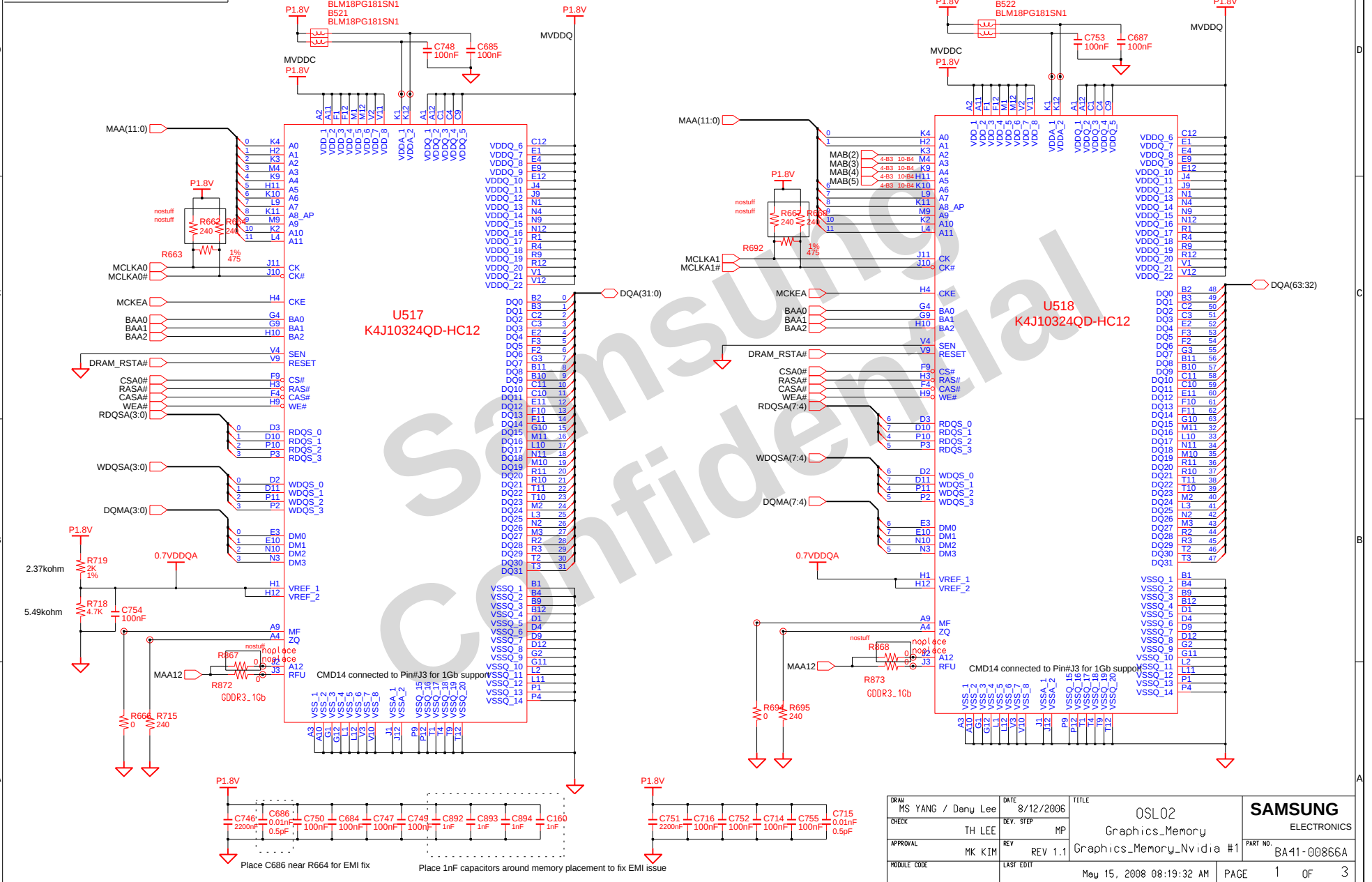


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CHECK	TH LEE	DEV. STEP	MP		EXT NB9X	
APPROVAL	MK KIM	REV	REV 1.1		NB9X POWER RAIL	PART NO. BA11-00866A
MODULE CODE		LAST EDIT				

May 15, 2008 08:19:32 AM PAGE 5 OF 5

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A-channel



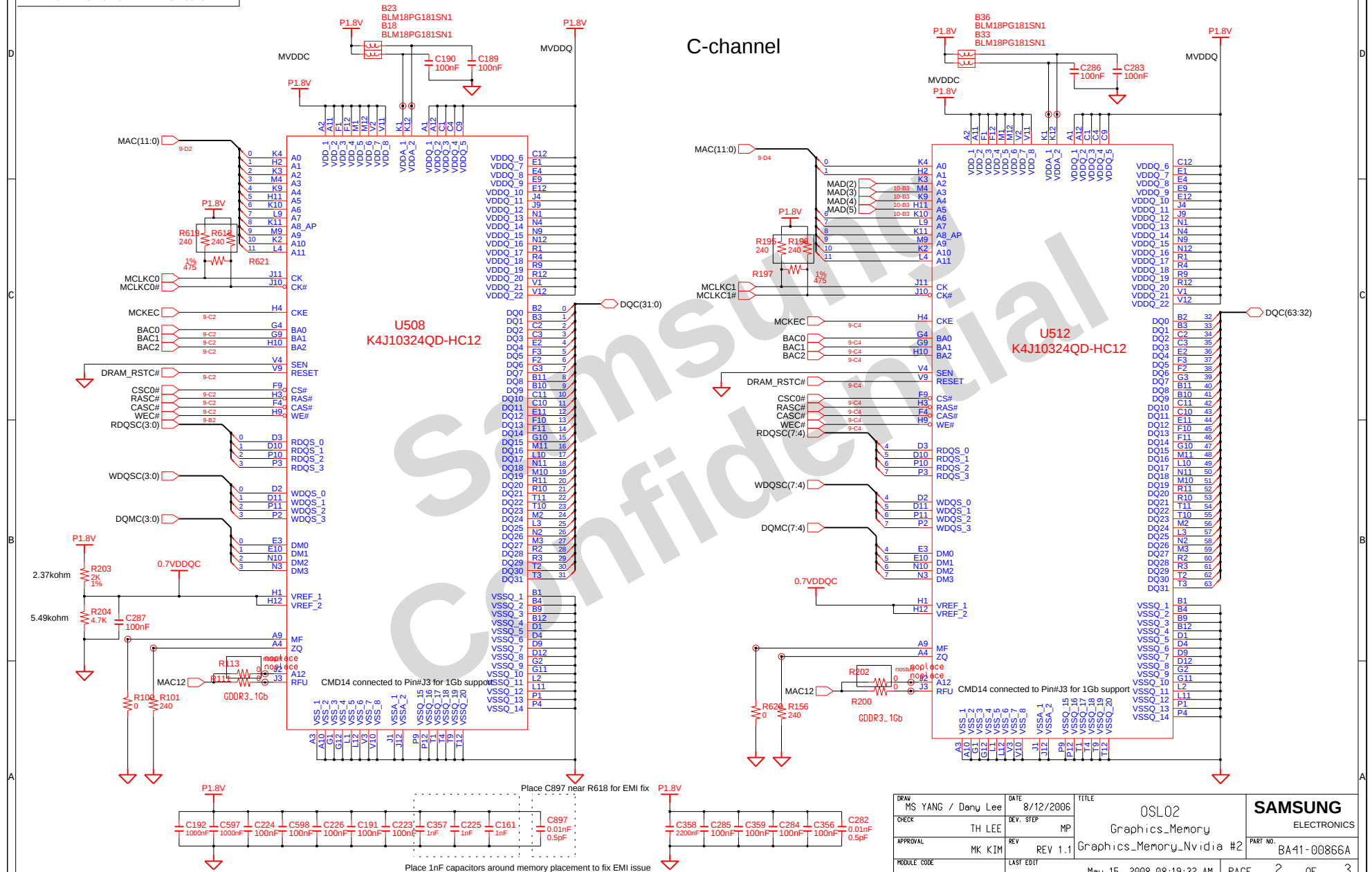
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APPROVAL MK KIM	REV REV 1.1	Graphics_Memory_Nvidia #1		
MODULE CODE		PART NO. BA41-00866A		
LAST EDIT		May 15, 2008 08:19:32 AM	PAGE	1 OF 3

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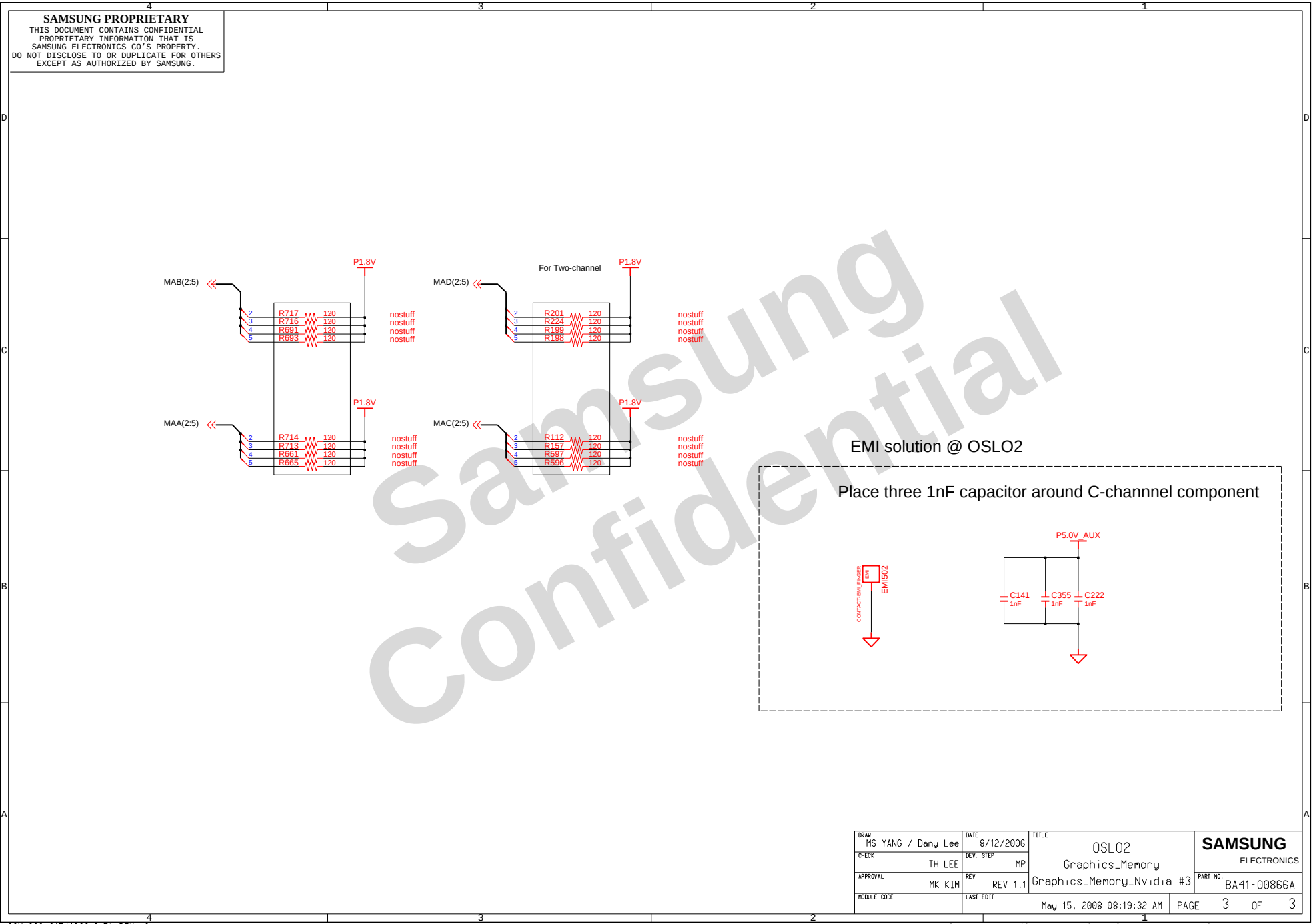
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This page is for "2channel-model".

C-channel

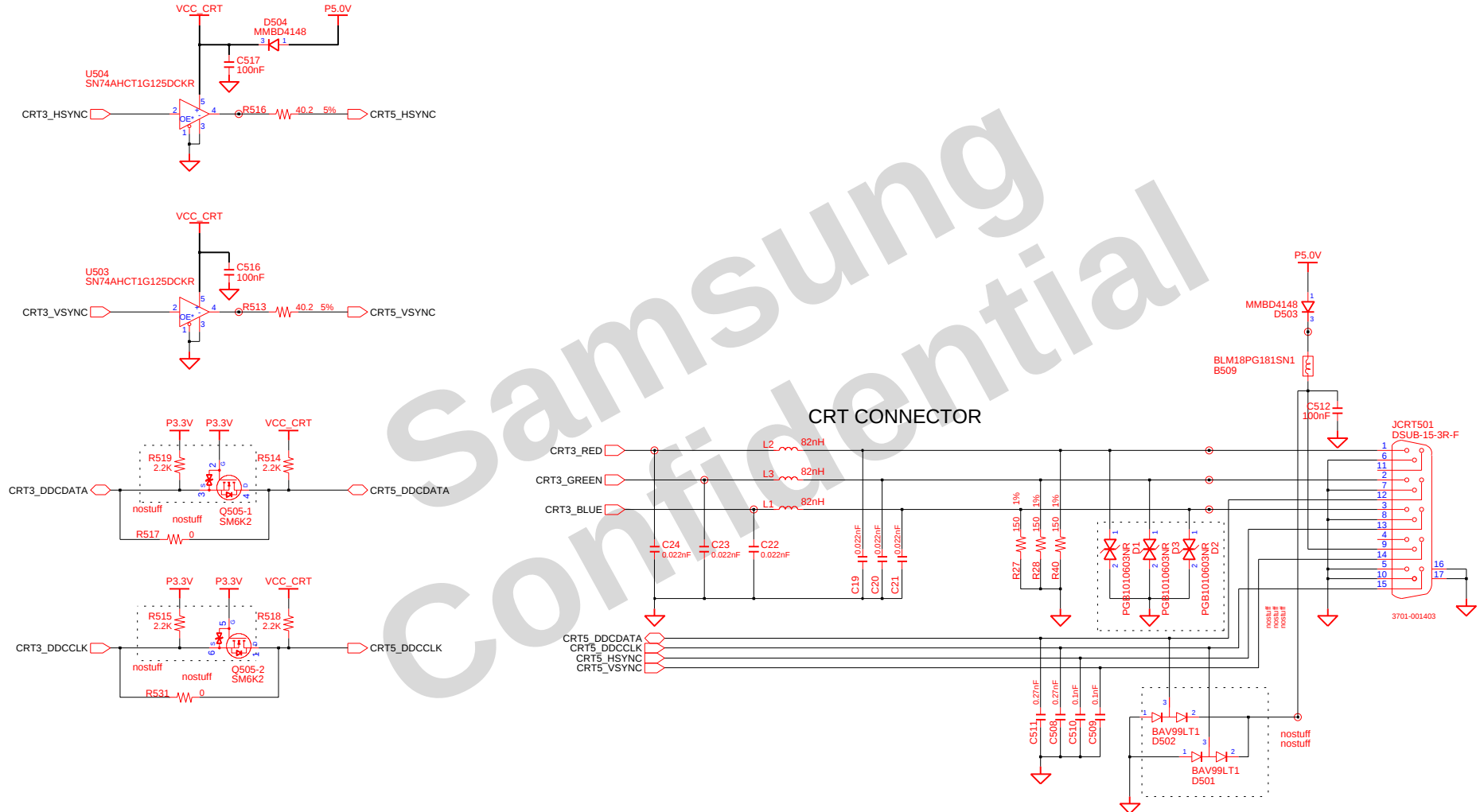


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APPROVAL	MK KIM	REV	REV 1.1	Graphics_Memory_Nvidia #2	PART NO.	BA41-00866A
MODULE CODE		LAST EDIT			May 15, 2008 08:19:32 AM	PAGE 2 OF 3



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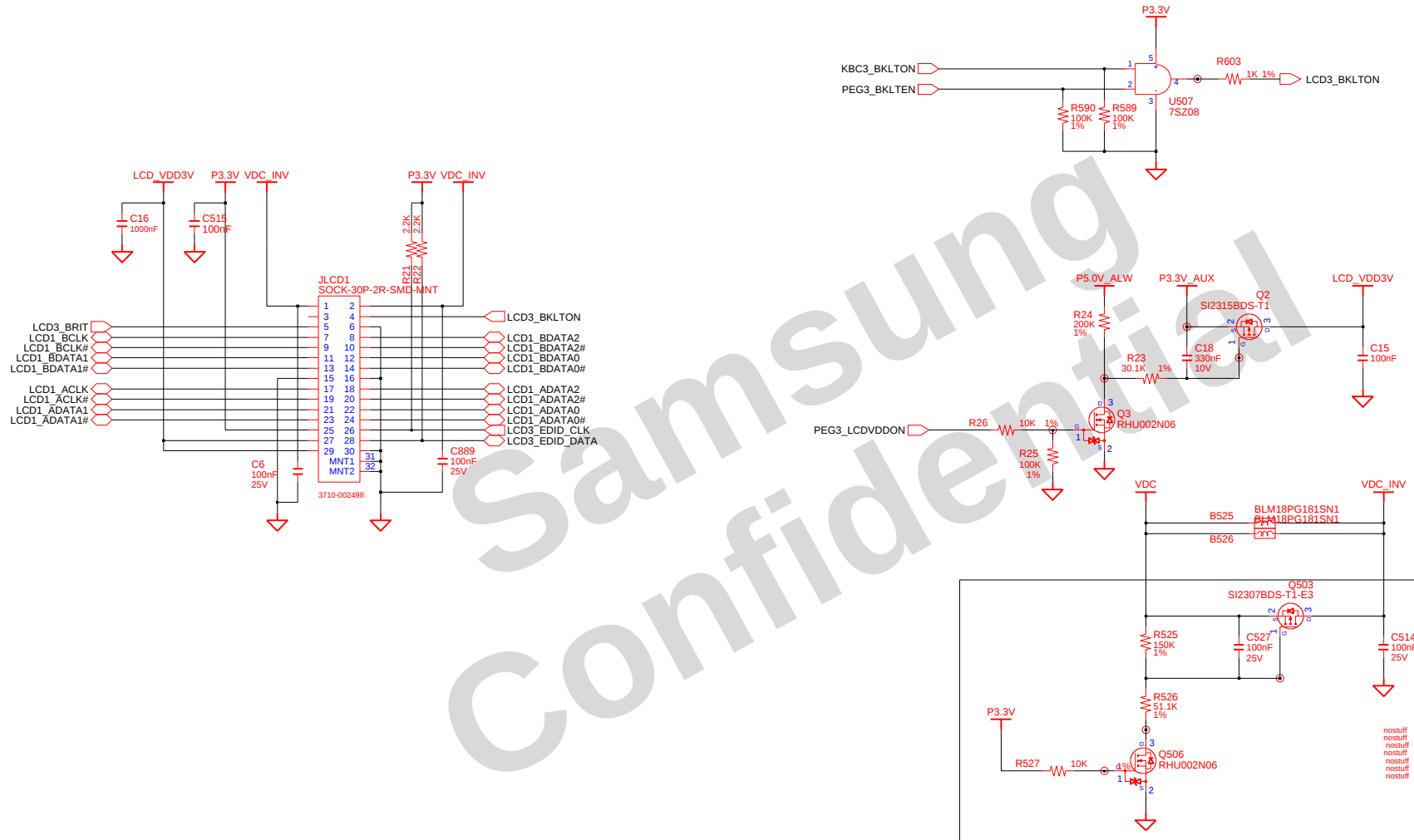


DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02 Interface_Circuit Graphics_IF_CRT	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK TH LEE	DEV. STEP MP	REV 1.1	
APPROVAL MK KIM	REV 1.1	LAST EDIT	
MODULE CODE	LAST EDIT		

May 15, 2008 08:19:32 AM PAGE 1 OF 3

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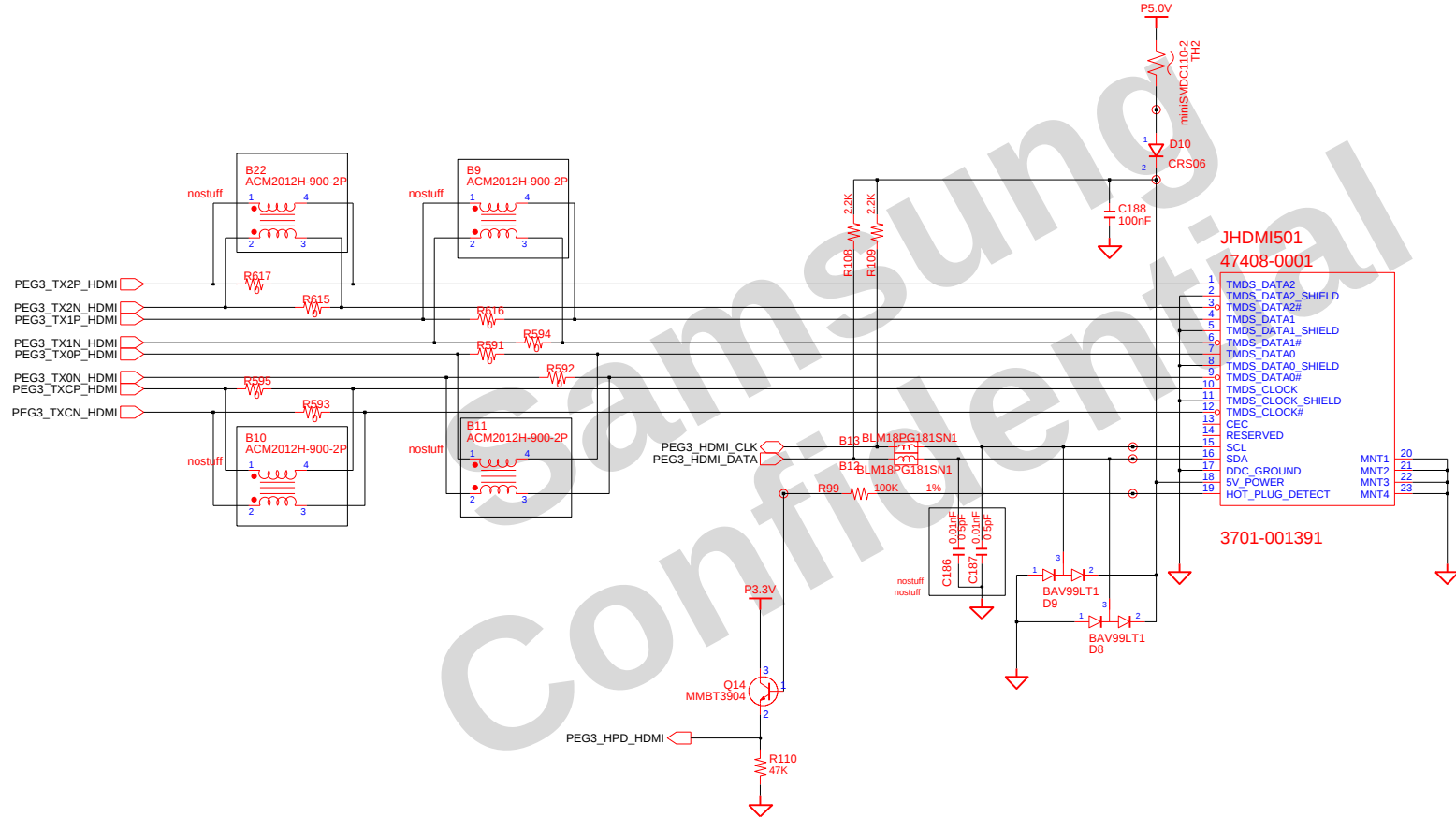
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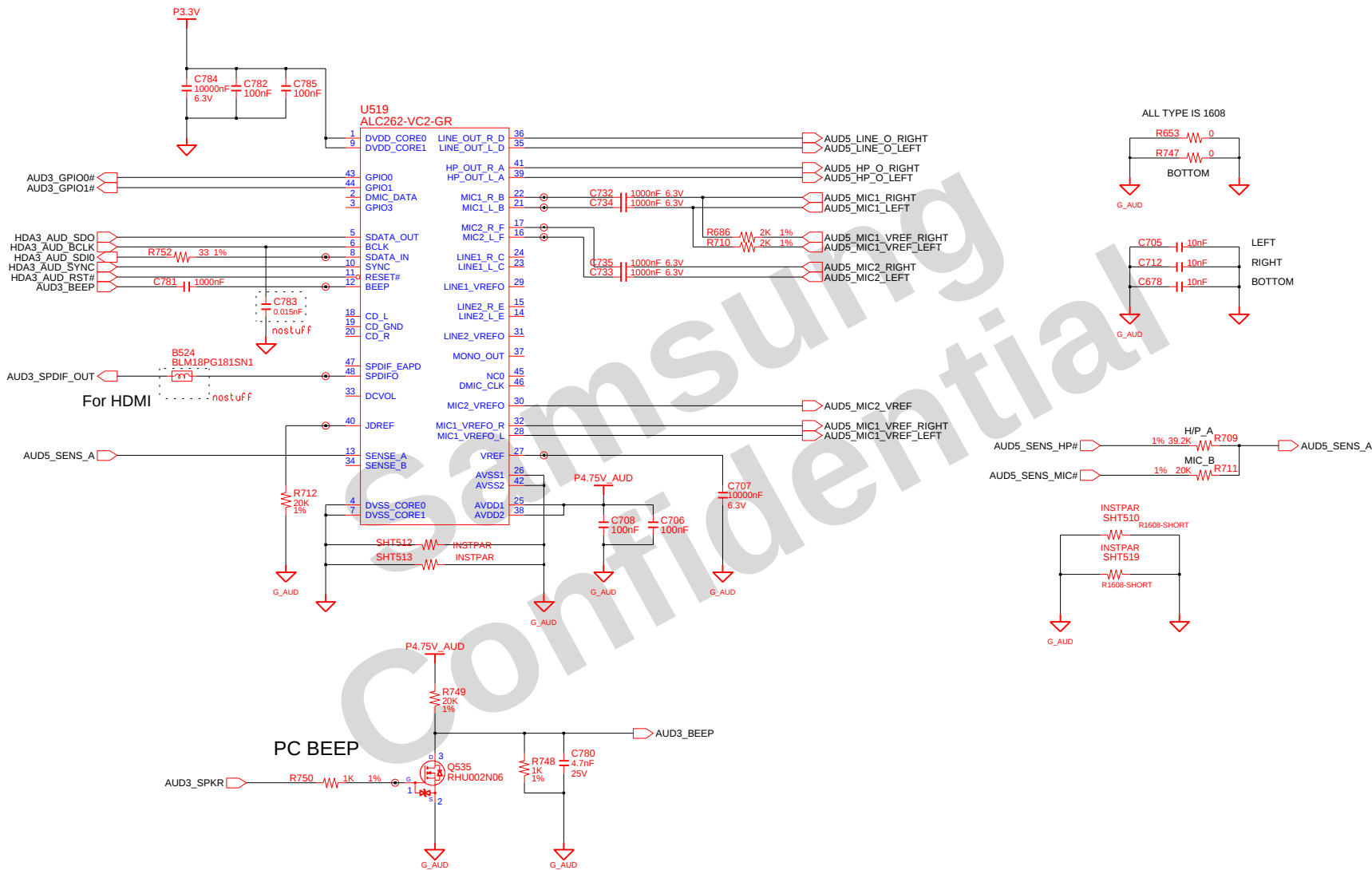
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CHECK	TH LEE	DEV. STEP	MP			
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MODULE CODE		LAST EDIT				
May 15, 2008 08:19:32 AM						PAGE 12 of 12

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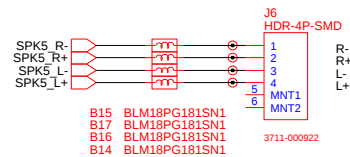
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DRAW MS YANG / Dany Lee	DATE 8/17/2007	TITLE OSL02 UNDEFINED	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK TH LEE	DEV. STEP MP		
APPROVAL MK KIM	REV REV 1.1		
MODULE CODE	LAST EDIT		
May 15, 2008 08:19:32 AM			PAGE 13 of 13



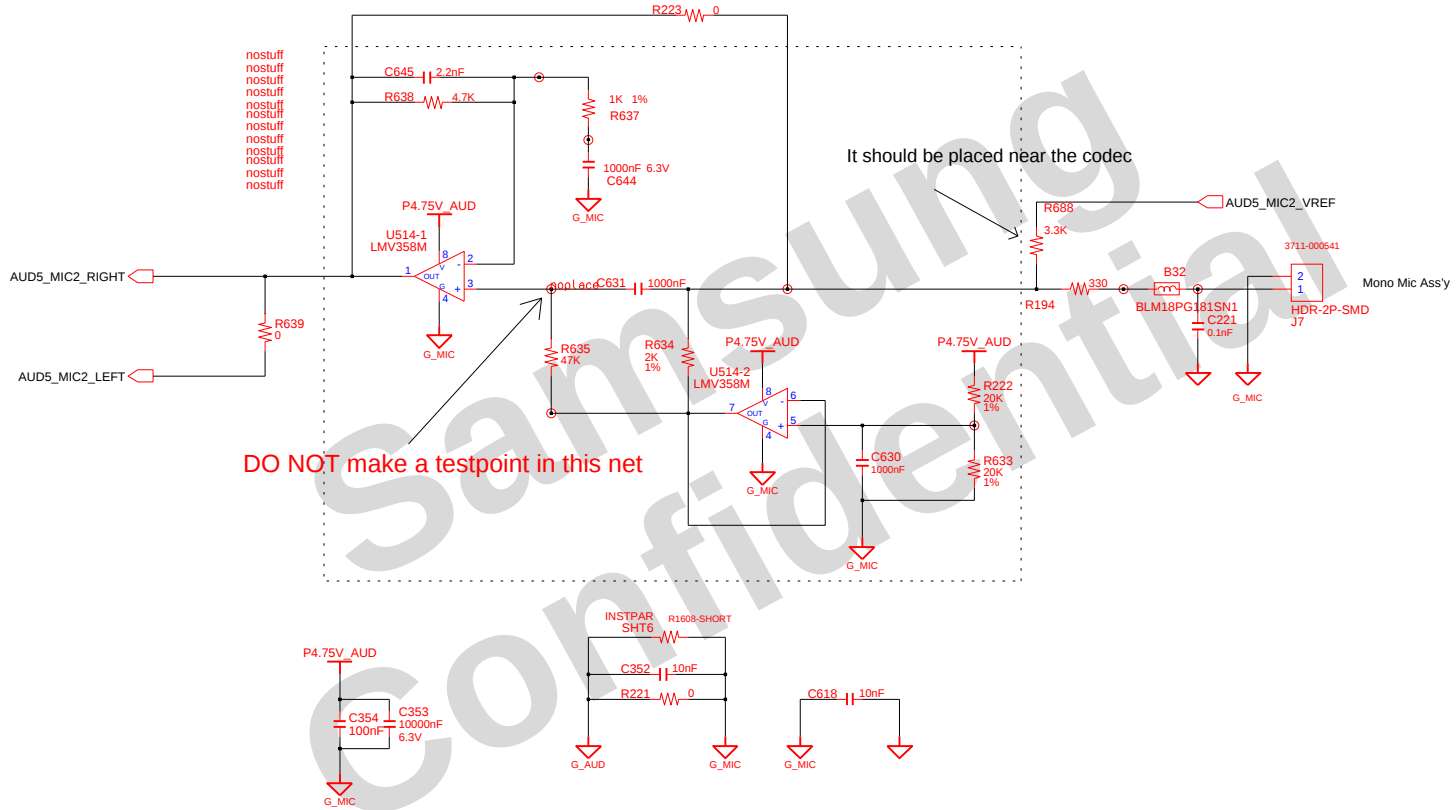
DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02	SAMSUNG ELECTRONICS PART NO. BA41-00866A
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APPROVAL MK KIM	REV REV 1.1	HDA_Codemc_Alc262 #1	
MODULE CODE undefined	LAST EDIT		
May 15, 2008 08:19:32 AM		PAGE 1 OF 5	



NAME MS YANG / Dany Lee		DATE 8/12/2006		TITLE OSL02 HDA_Codec_Alc262 HDA_Codec_Alc262 #2			
CHECK TH LEE		DEV. STEP MP					
APPROVAL MK KIM		REV REV 1.1		PART NO. 8A41-00866A			
MODULE CODE		LAST EDIT		May 15, 2008 08:19:32 AM		PAGE	2 OF 5

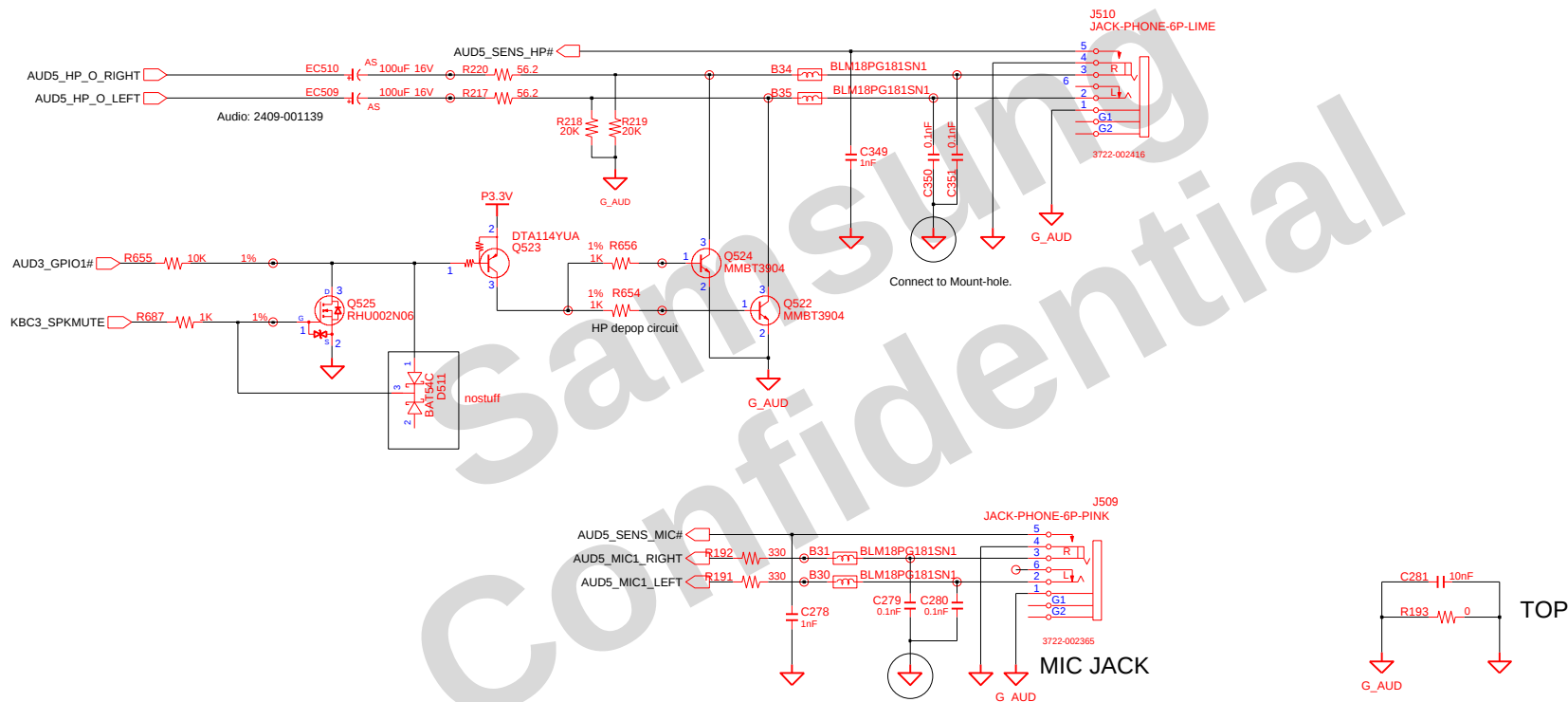
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DRW	MS YANG / Dany Lee	DATE	8/12/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP		HDA_Codec_Alc262	
APPROVAL	MK KIM	REV	1.1		HDA_Codec_Alc262 #3	PART NO.
MODULE CODE	undefined	LAST EDIT				BA11-00866A
				May 15, 2008 08:19:32 AM	PAGE	3 OF 5

HEADPHONE

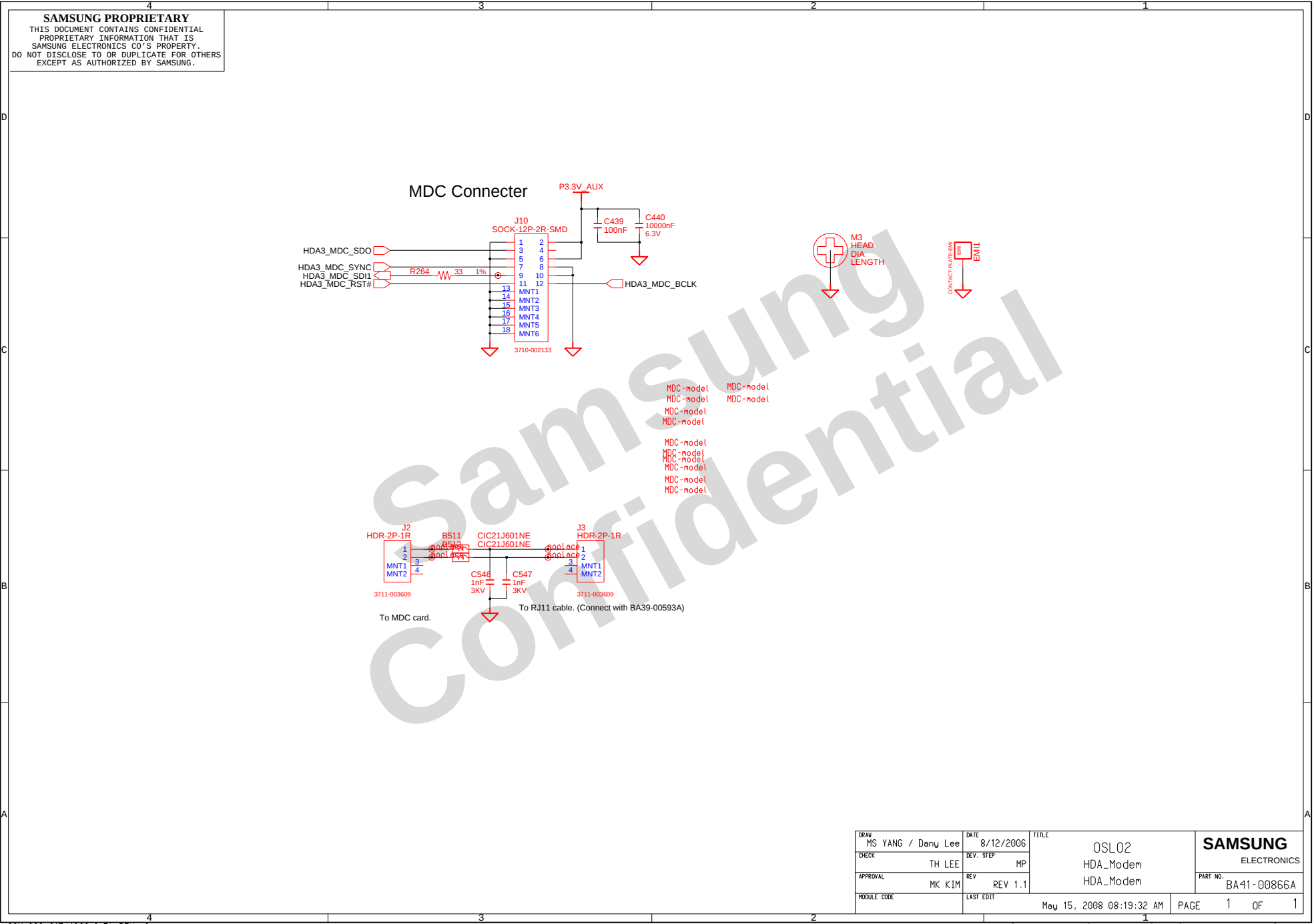


The traces led to Audio Jacks have the width over 10mil

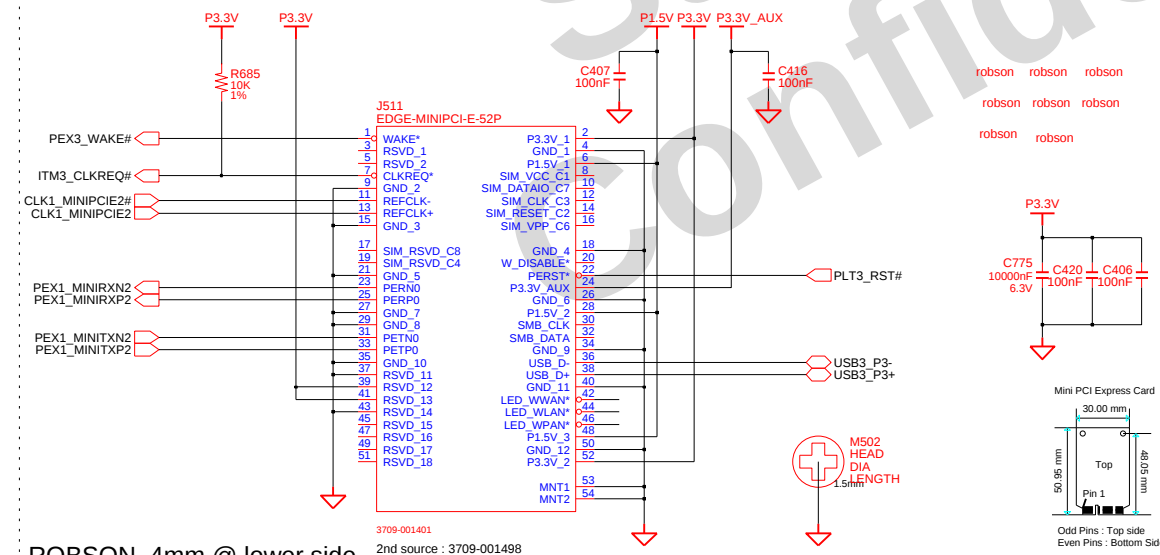
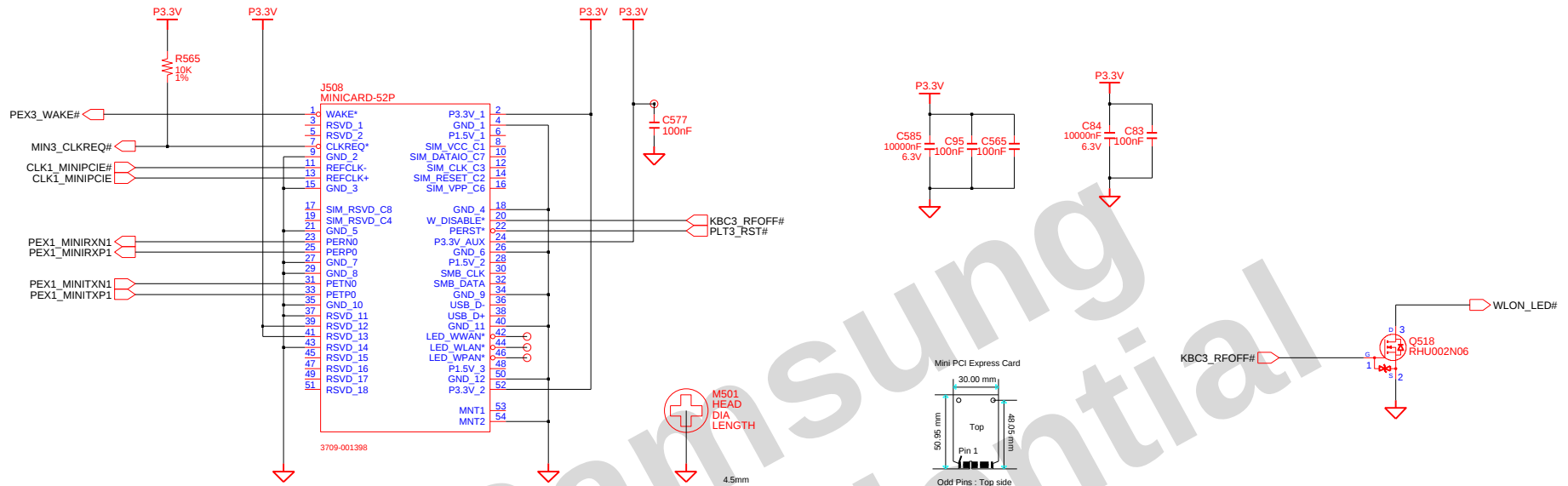
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APPROVAL	MK KIM	REV	REV 1.1		HDA_Codec_A1c262 #4	PART NO.	BA41-00866A
MODULE CODE		LAST EDIT	May 15, 2008 08:19:32 AM			PAGE	4 OF 5

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DSN MS YANG / Dany Lee		DATE 8/12/2006		TITLE OSLO2 HDA_Codec_Alc262 HDA_Codec_Alc262 #5			
CHECK TH LEE		DEV. STEP MP					
APPROVAL MK KIM		REV REV 1.1		PART NO.		BA41-00866A	
MODULE CODE undefined		LAST EDIT May 15, 2008 08:19:32 AM		PAGE		5 OF 5	



WLAN, 7mm @ Upper side

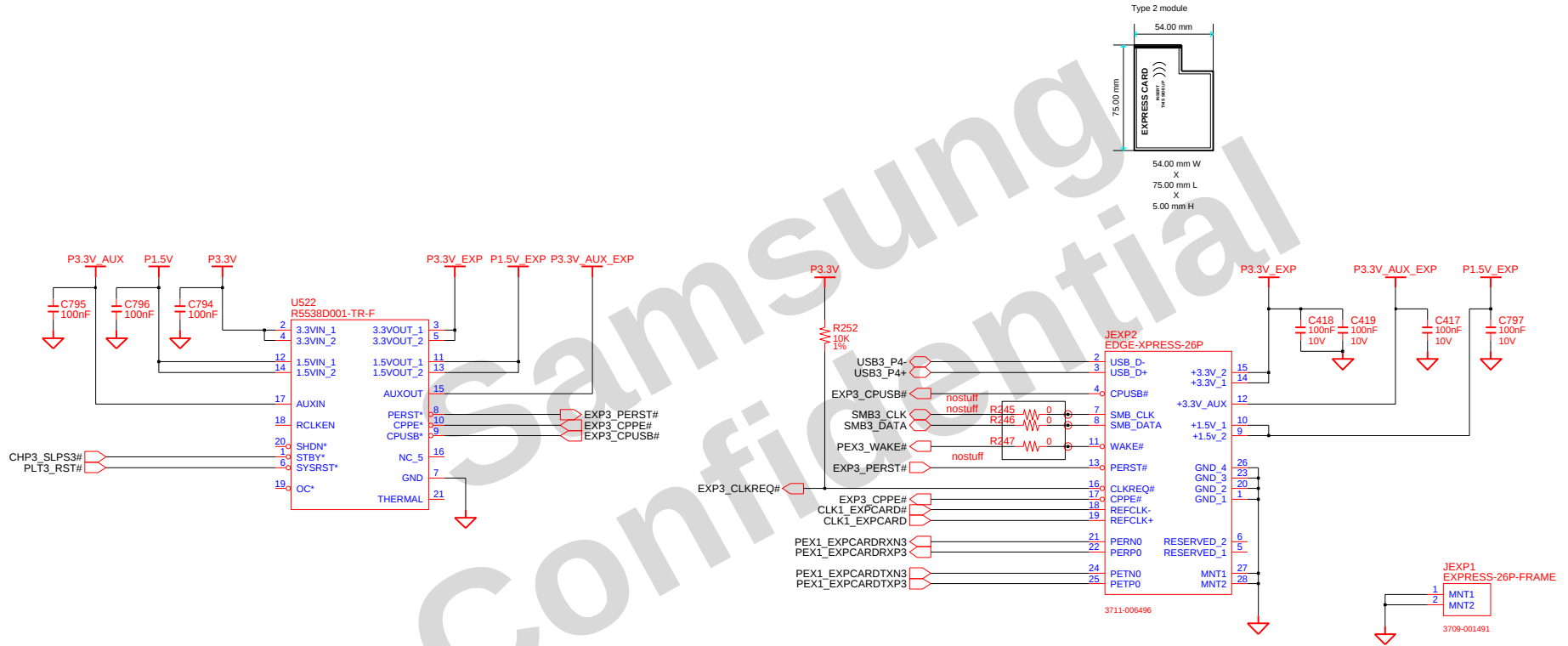


ROBSON, 4mm @ lower side

DRAW	MS YANG / Dany Lee	DATE	8/12/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP	PCIE_Minicard_Slot	PART NO.	
APPROVAL	MK KIM	REV	REV 1.1	PCIE_Minicard_Slot	BA41-00866A	
MODULE CODE	undefined	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE	1	OF 1

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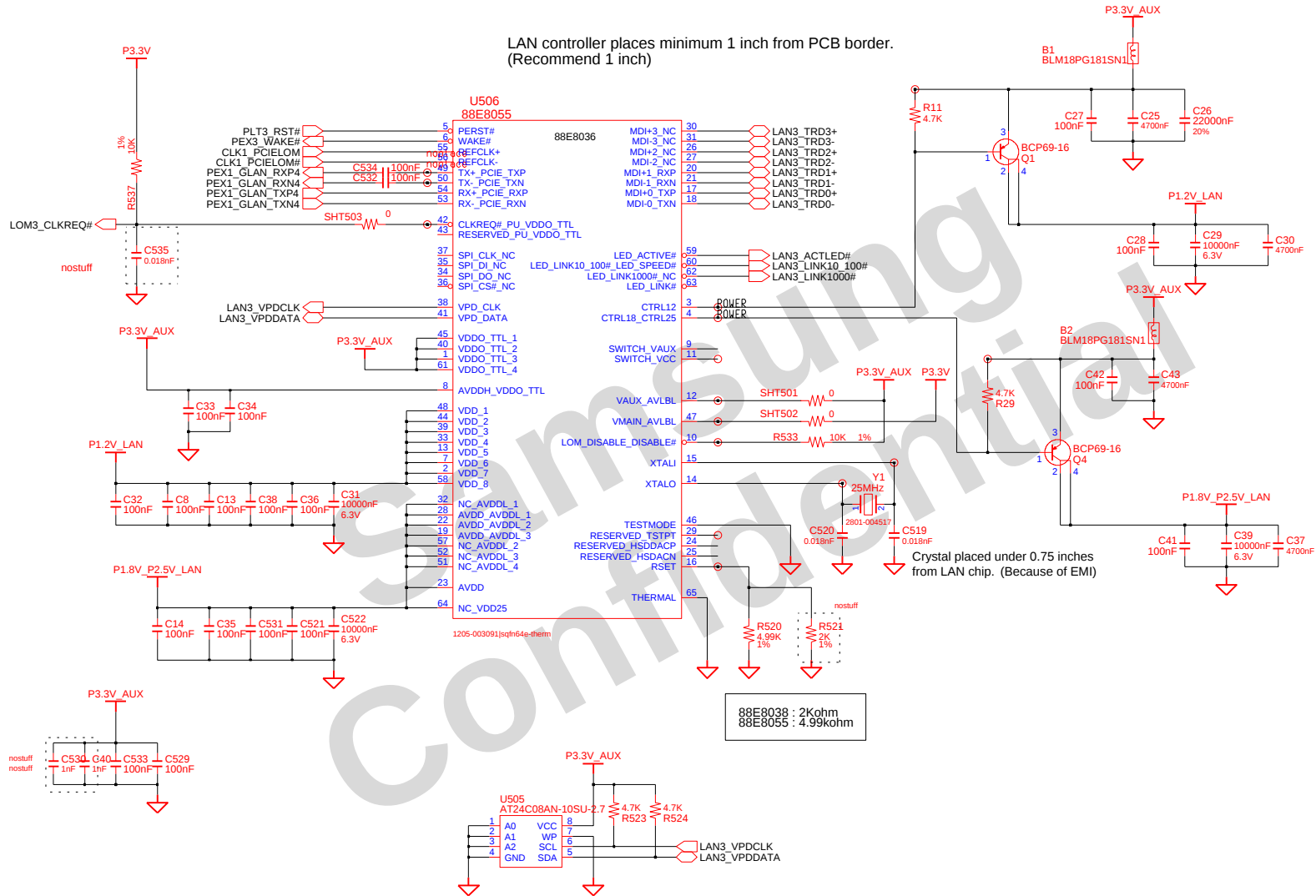


DRW MS YANG / Dany Lee	DATE	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK TH LEE	DEV. STEP MP			
APPROVAL MK KIM	REV REV 1.1			PART NO. BA11-00866A
MODULE CODE undefined	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE	OF

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LAN controller places minimum 1 inch from PCB border.
 (Recommend 1 inch)



Crystal placed under 0.75 inches
 from LAN chip. (Because of EMI)

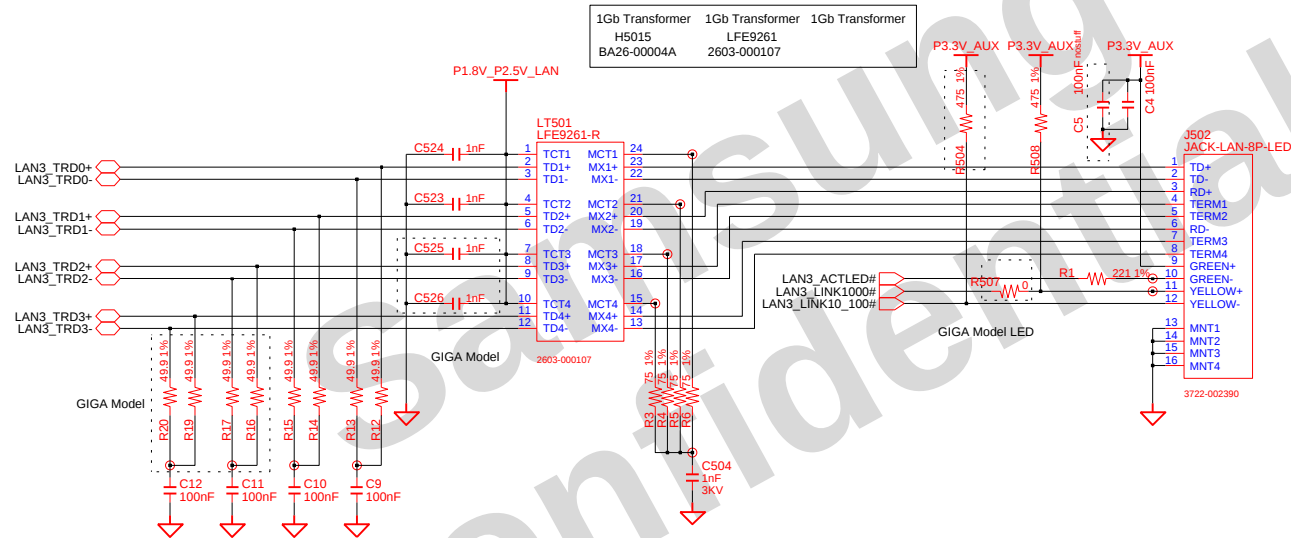
88E8038 : 2Kohm
 88E8055 : 4.99kohm

DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK TH LEE	DEV. STEP MP	LAN_Marvell_8055	
APPROVAL MK KIM	REV REV 1.1	LAN_Marvell_8055	
MODULE CODE	LAST EDIT		

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The distance between LAN controller
and transformer is designed to extend less than two inches.

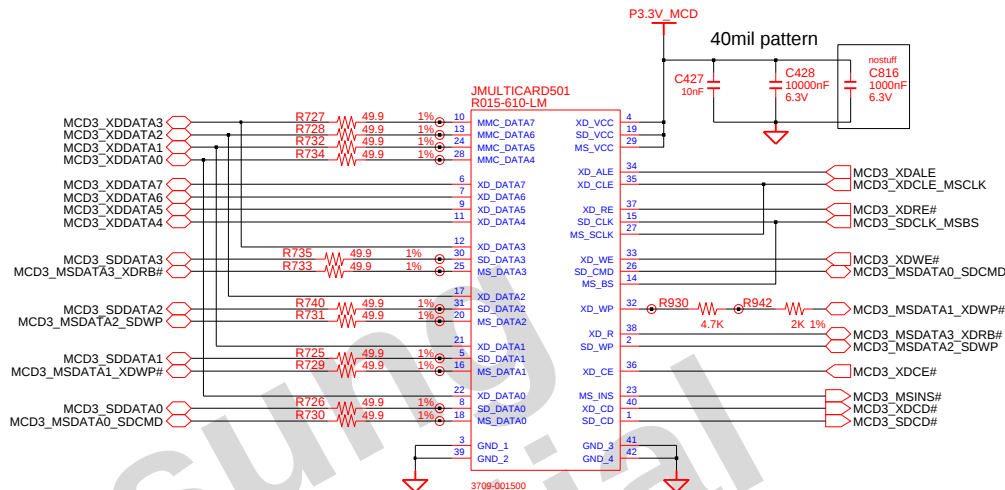


Place near to the Marvell chip.

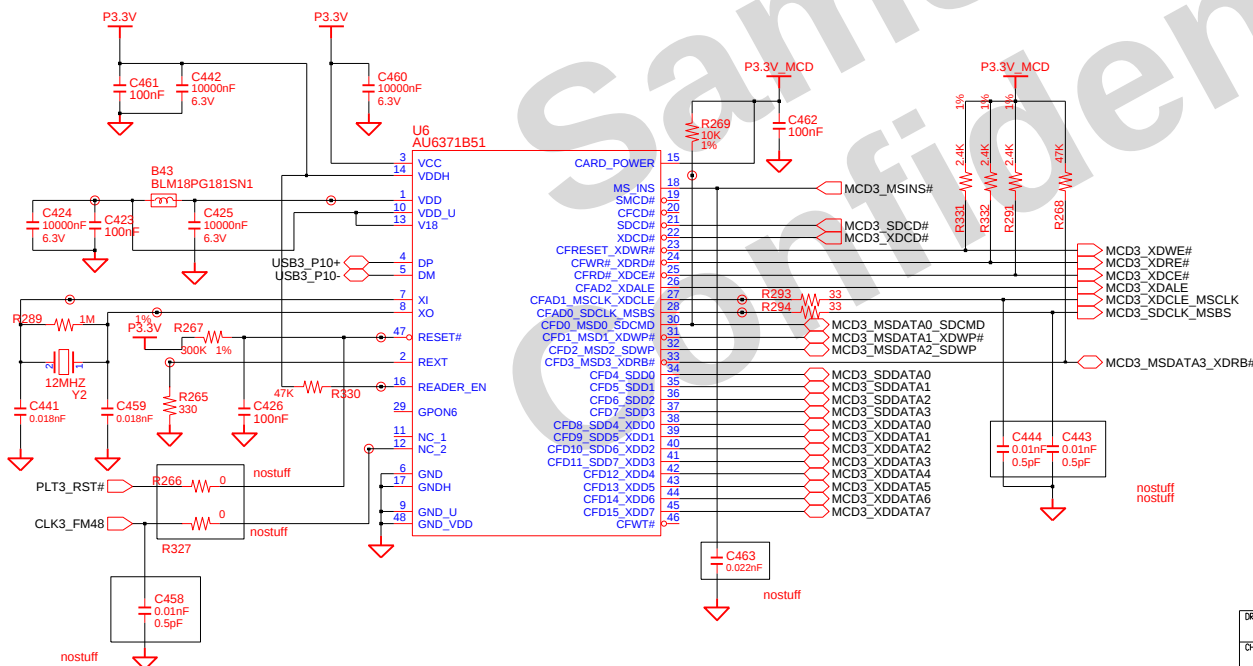
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APPROVAL MK KIM	REV REV 1.1	LAN_Marvell_8055	
MODULE CODE	LAST EDIT		
May 15, 2008 08:19:32 AM			PAGE 2 OF 2

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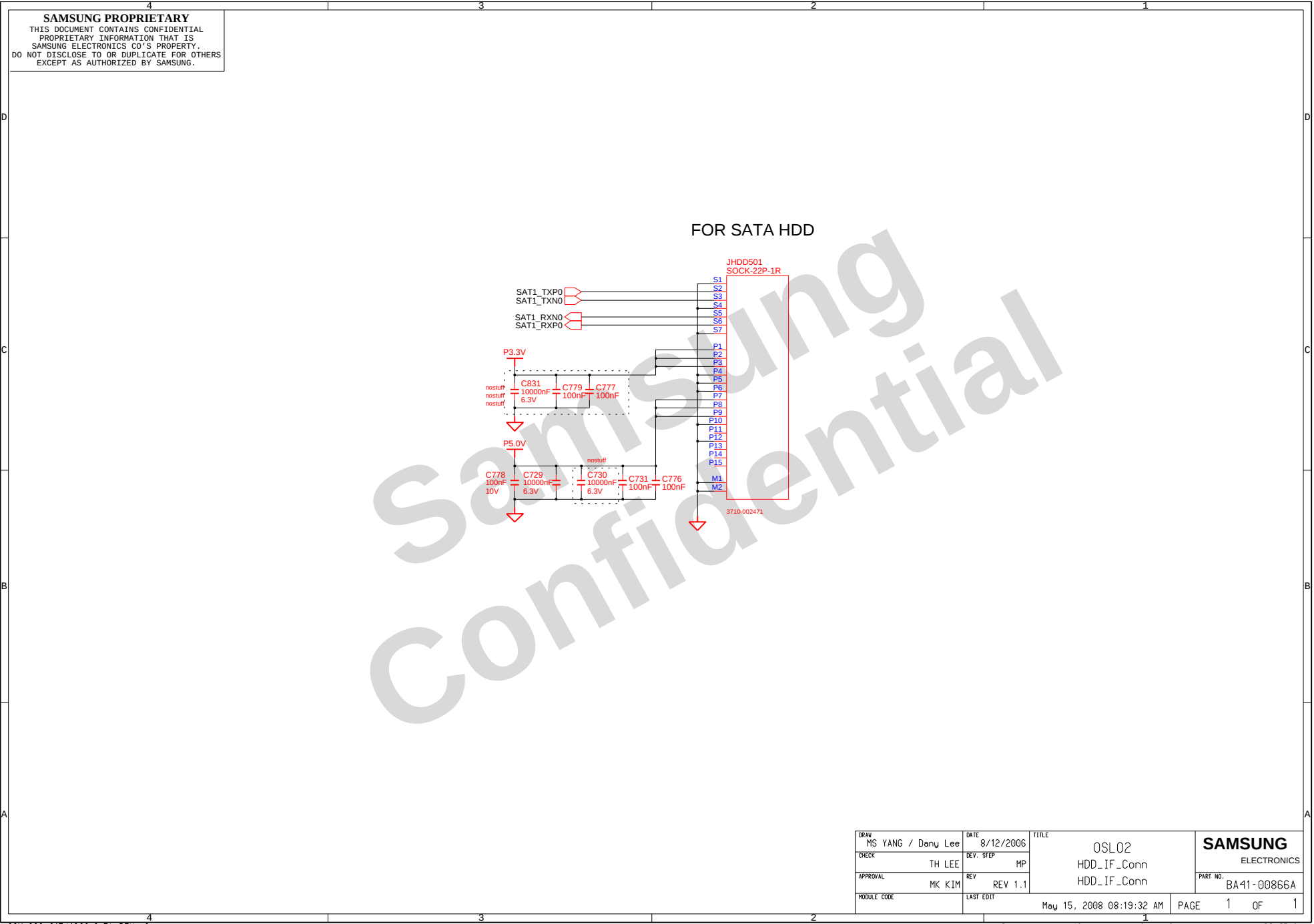
P3.3V_MCD distance between Controller and socket should be less than 2 inches

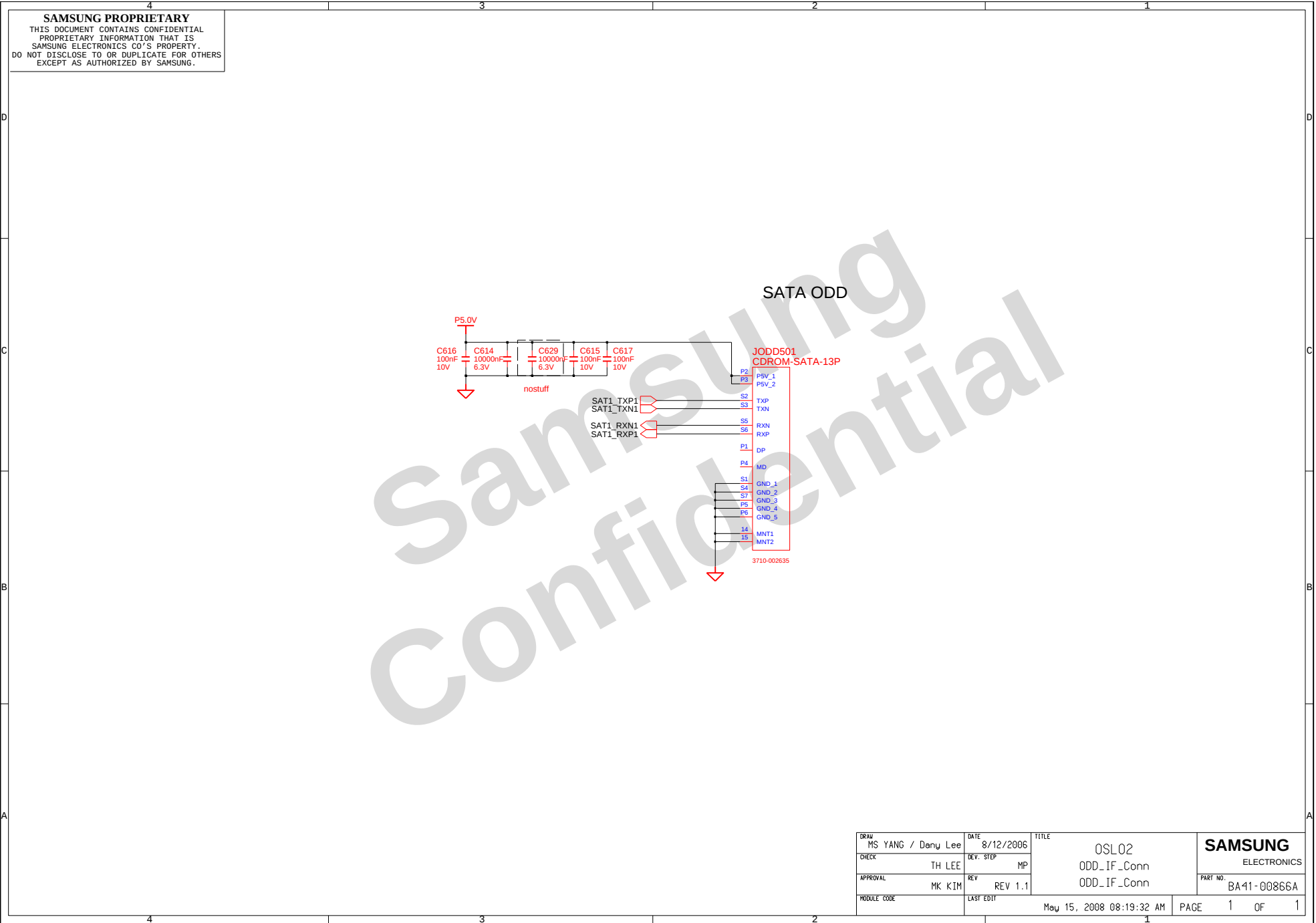


40 mil trace for medica card socket ground



DRAW MS YANG / Dany Lee	DATE 8/17/2007	TITLE OSL02 UNDEFINED		
CHECK TH LEE	REV. STEP MP			
APPROVAL MK KIM	REV REV 1.1	PART NO. BA41-00866A		
MODULE CODE	LAST EDIT May 15, 2008 08:19:32 AM	PAGE 1	Undefined	



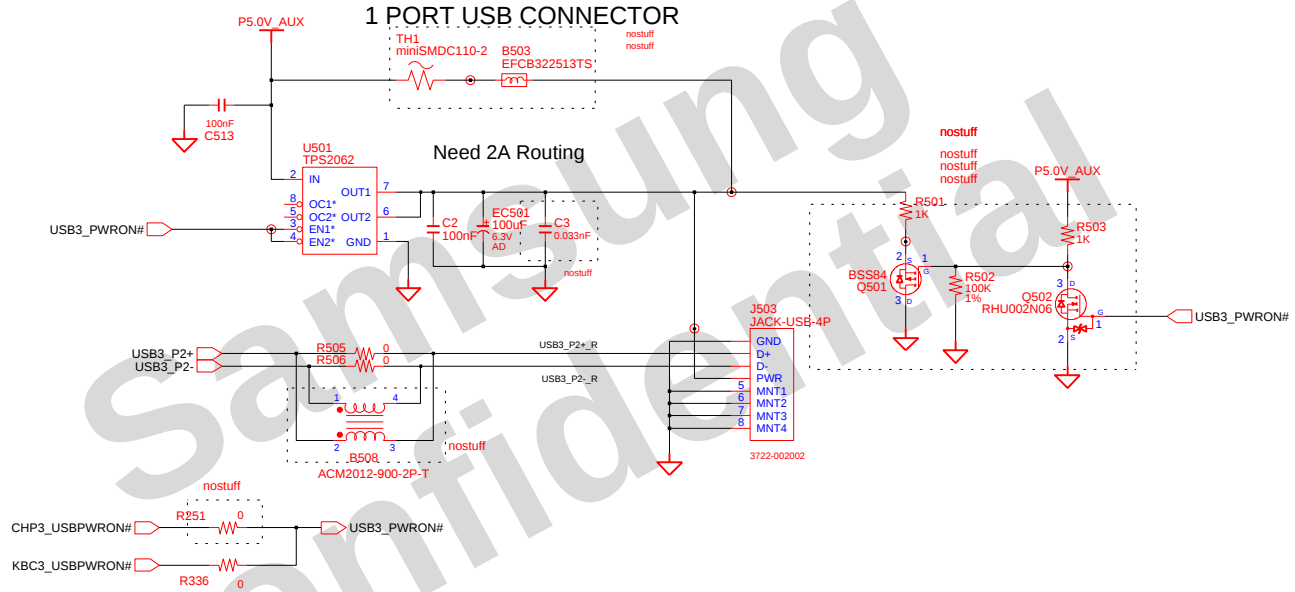


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DRW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02	SAMSUNG ELECTRONICS
CHECK TH LEE	DEV. STEP MP	ODD_IF_Conn	
APPROVAL MK KIM	REV REV 1.1	ODD_IF_Conn	PART NO. BA41-00866A
MODULE CODE	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE 1 OF 1

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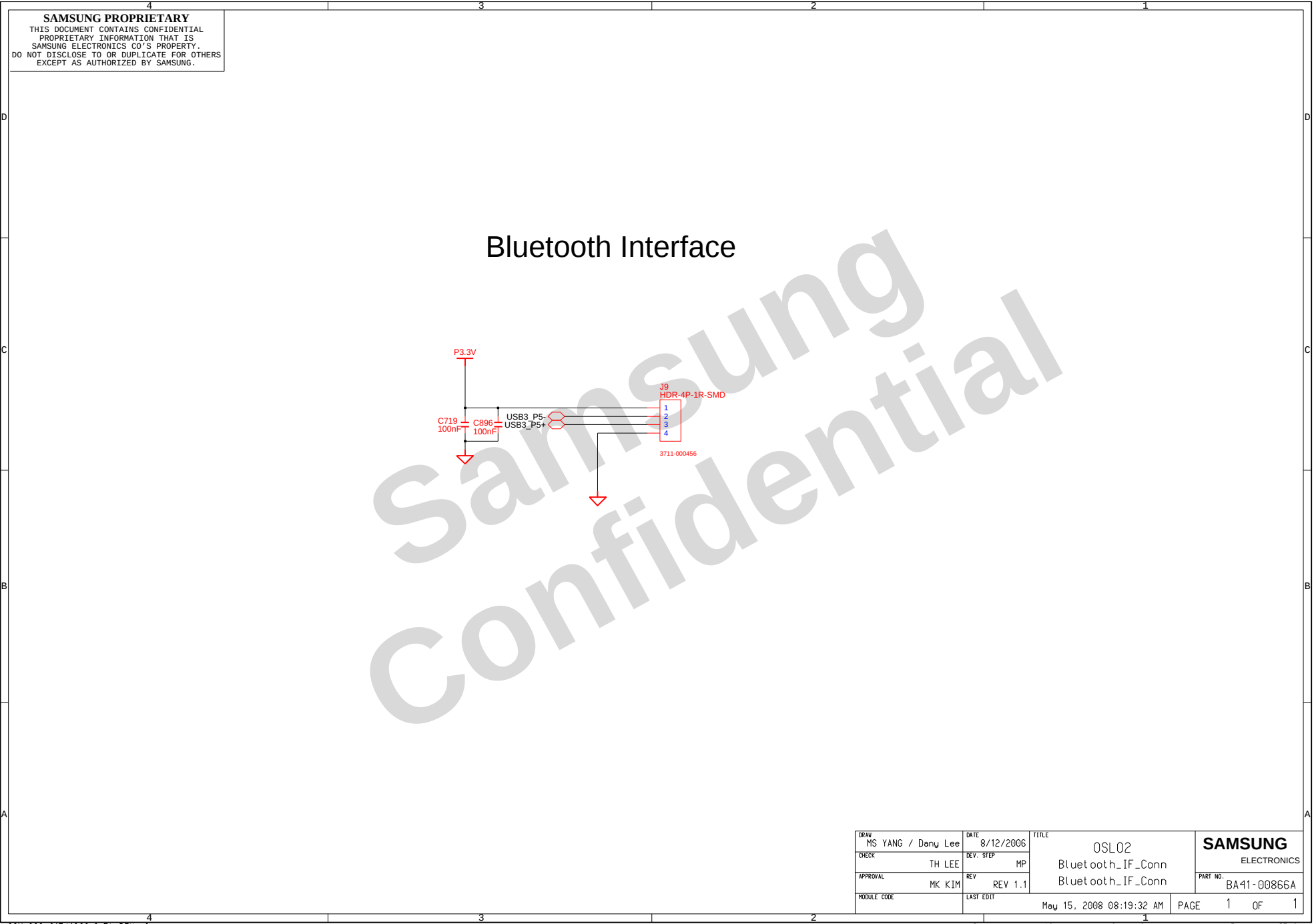
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DRW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02 USB_1Port USB_1Port	SAMSUNG ELECTRONICS
CHECK TH LEE	DEV. STEP MP		PART NO. BA11-00866A
APPROVAL MK KIM	REV REV 1.1		
MODULE CODE	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE 1 OF 1

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D:/users/mobile16/mentor/oslo2/oslo2_pr/design_blocks/USB_2Port
SRP Sheet Number: 55 of 76



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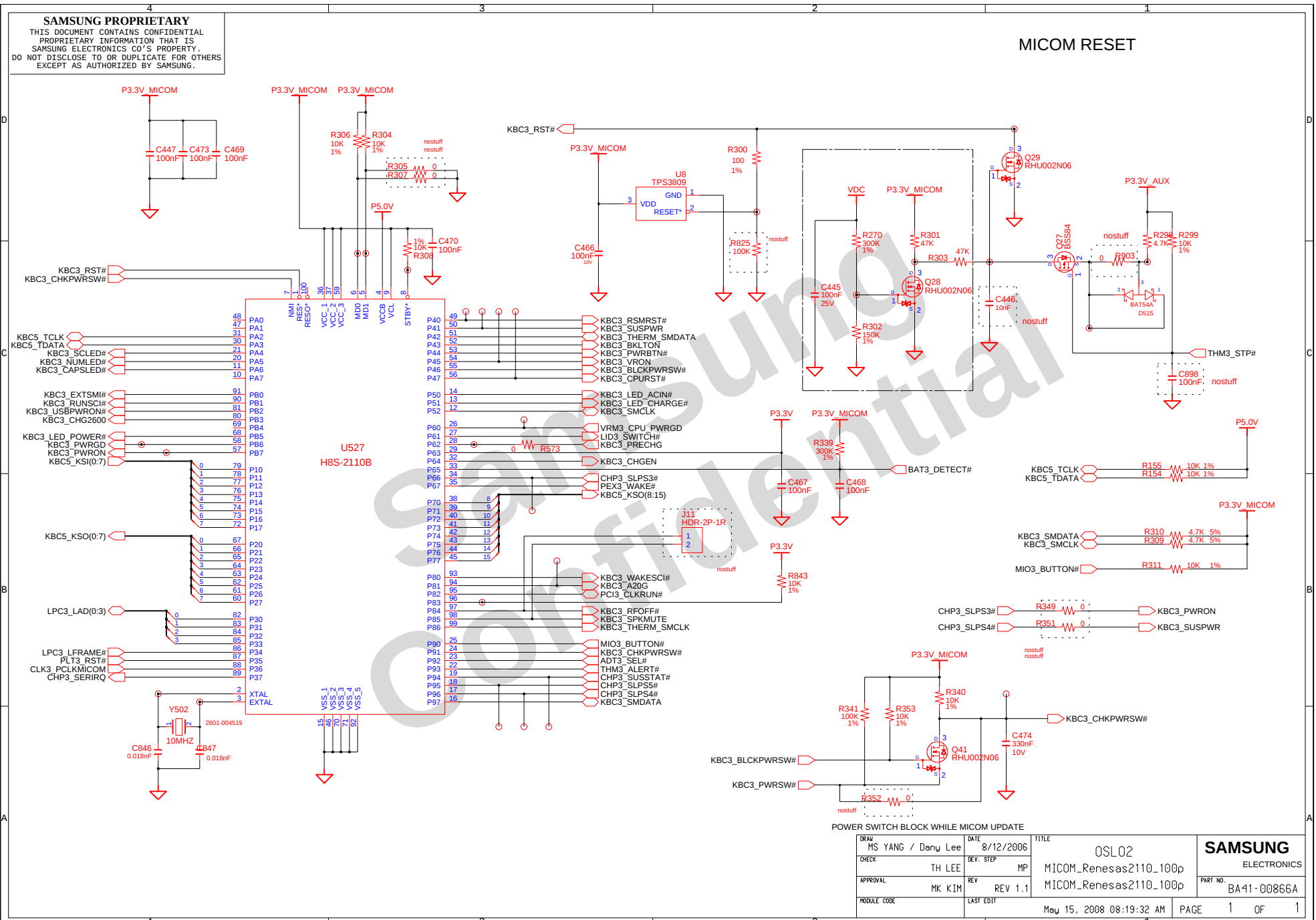
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APPROVAL	MK KIM	REV	REV 1.1		Camera_IF_Conn	PART NO.	BA41-00866A
MODULE CODE		LAST EDIT		May 15, 2008 08:19:32 AM	PAGE	1	OF 1



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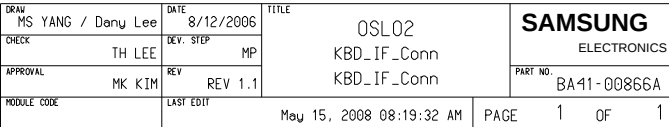
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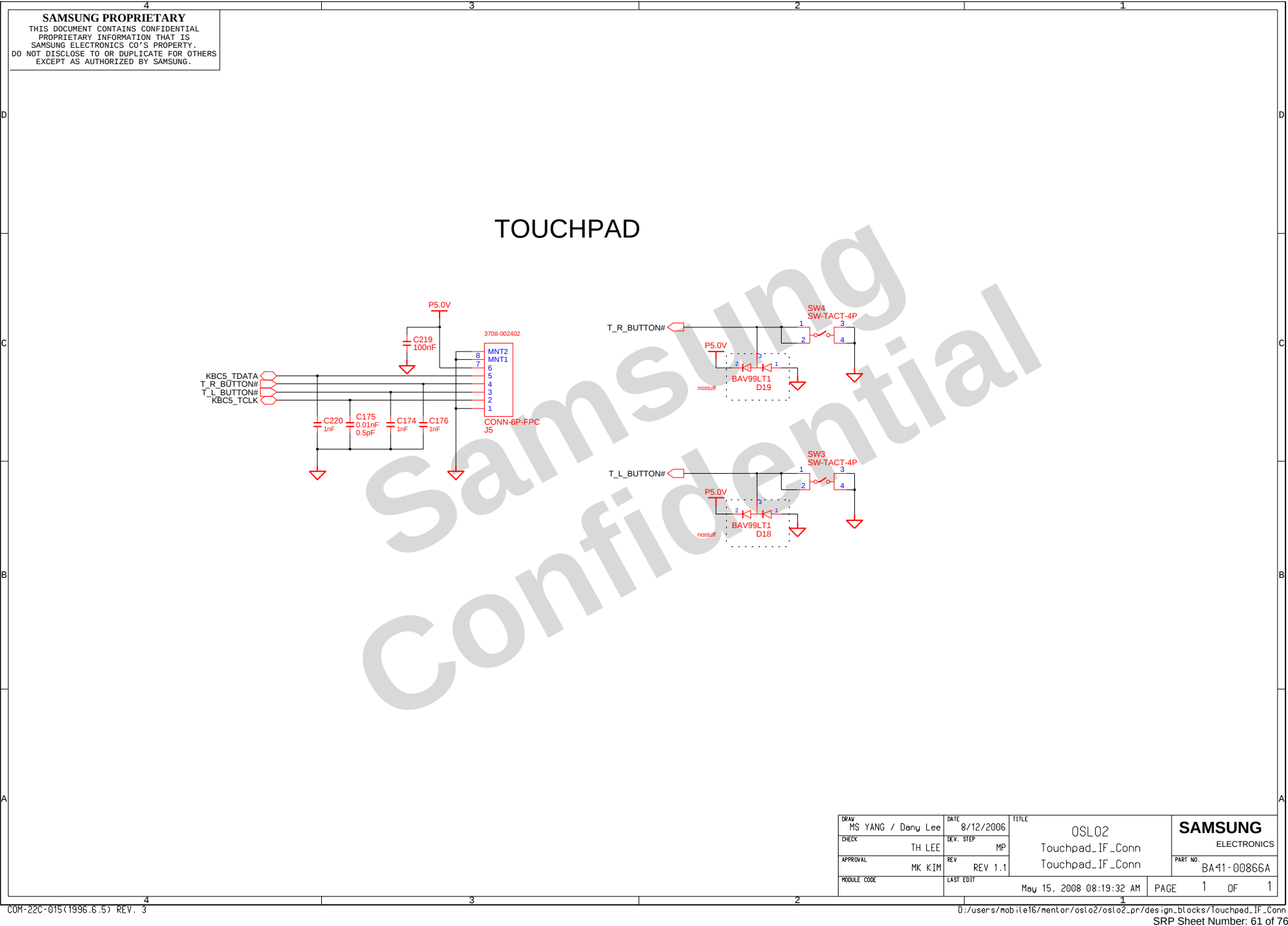


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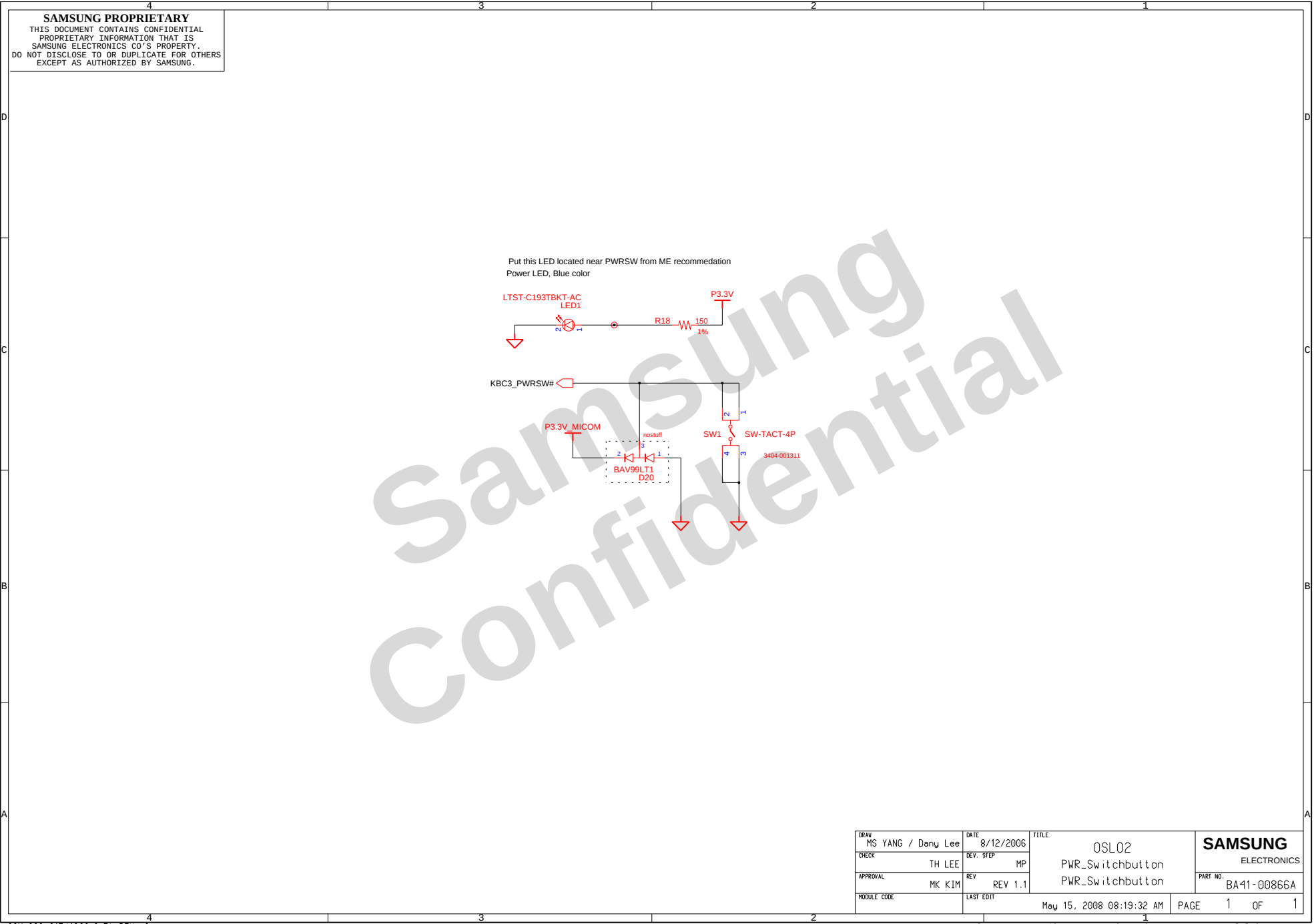
MICOM RESET

KEYBOARD





DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02 Touchpad_IF_Conn Touchpad_IF_Conn	SAMSUNG ELECTRONICS PART NO. BA41-00866A
CHECK TH LEE	DEV. STEP MP	REV REV 1.1	
APPROVAL MK KIM	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE 1 OF 1
MODULE CODE			



DRAW	MS YANG / Dany Lee	DATE	8/12/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP	PWR_Switchbutton	PWR_Switchbutton	
APPROVAL	MK KIM	REV	REV 1.1	PART NO. BA41-00866A		
MODULE CODE	LAST EDIT		May 15, 2008 08:19:32 AM		PAGE 1 OF 1	

COM-22C-015(1996.6.5) REV. 3

D:/users/mobile16/mentor/oslo2/oslo2_pr/design_blocks/PWR_Switchbutton

SRP Sheet Number: 62 of 76

4

3

2

1

D

C

B

A

4

3

2

1

COM-22C-015(1996.6.5) REV. 3

8/12/2006

8/12/2006

MS YANG / Dany Lee

TH LEE

MK KIM

DATE

DEV. STEP

REV

LAST EDIT

TITLE

OSL02

MIO_Switch

MIO_Switch

PAGE 1 OF 1

SAMSUNG ELECTRONICS

PART NO. BA41-00866A

May 15, 2008 08:19:32 AM

D:/users/nobile16/nentor/oslo2/oslo2_pr/design_blocks/MIO_Switch

SPP Sheet Number: 63 of 76

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MIO3_BUTTON#

P3.3V MICOM

BAV99LT1 D13

SW2

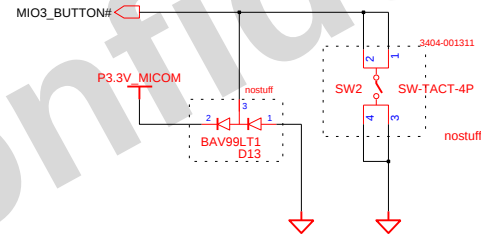
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nostuff

nostuff

3404-001311

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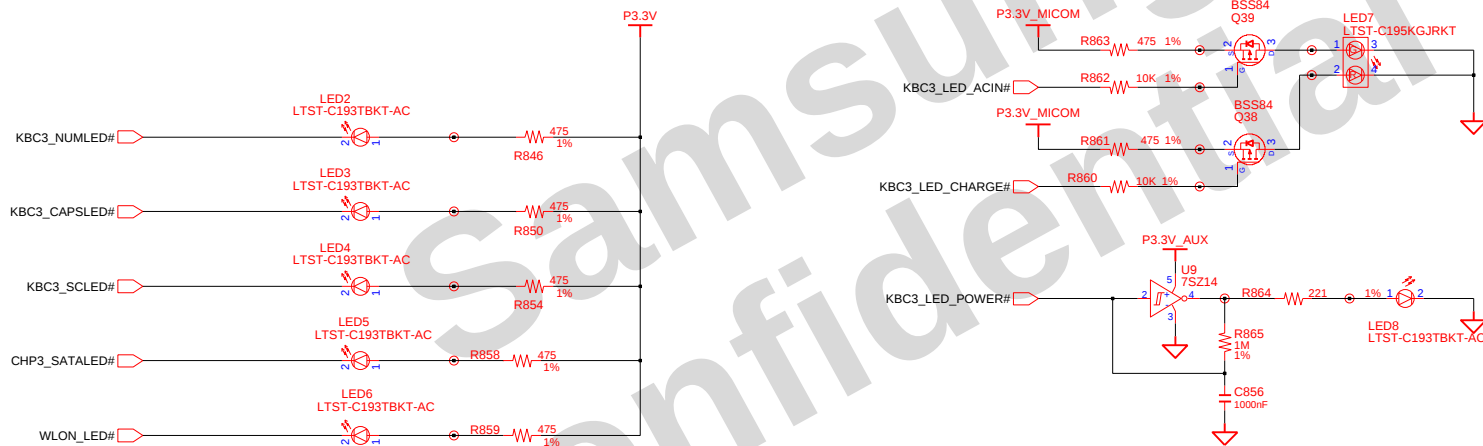


DRW	DATE	TITLE			
MS YANG / Dany Lee	8/12/2006	OSLO2			
CHECK	DEV. STEP	MP	MIO_Switch		PART NO.
TH LEE			MIO_Switch		
APPROVAL	REV	REV 1.1			BA41-00866A
MK KIM					
MODULE CODE	LAST EDIT	May 15, 2008 08:19:32 AM		PAGE	1 OF 1

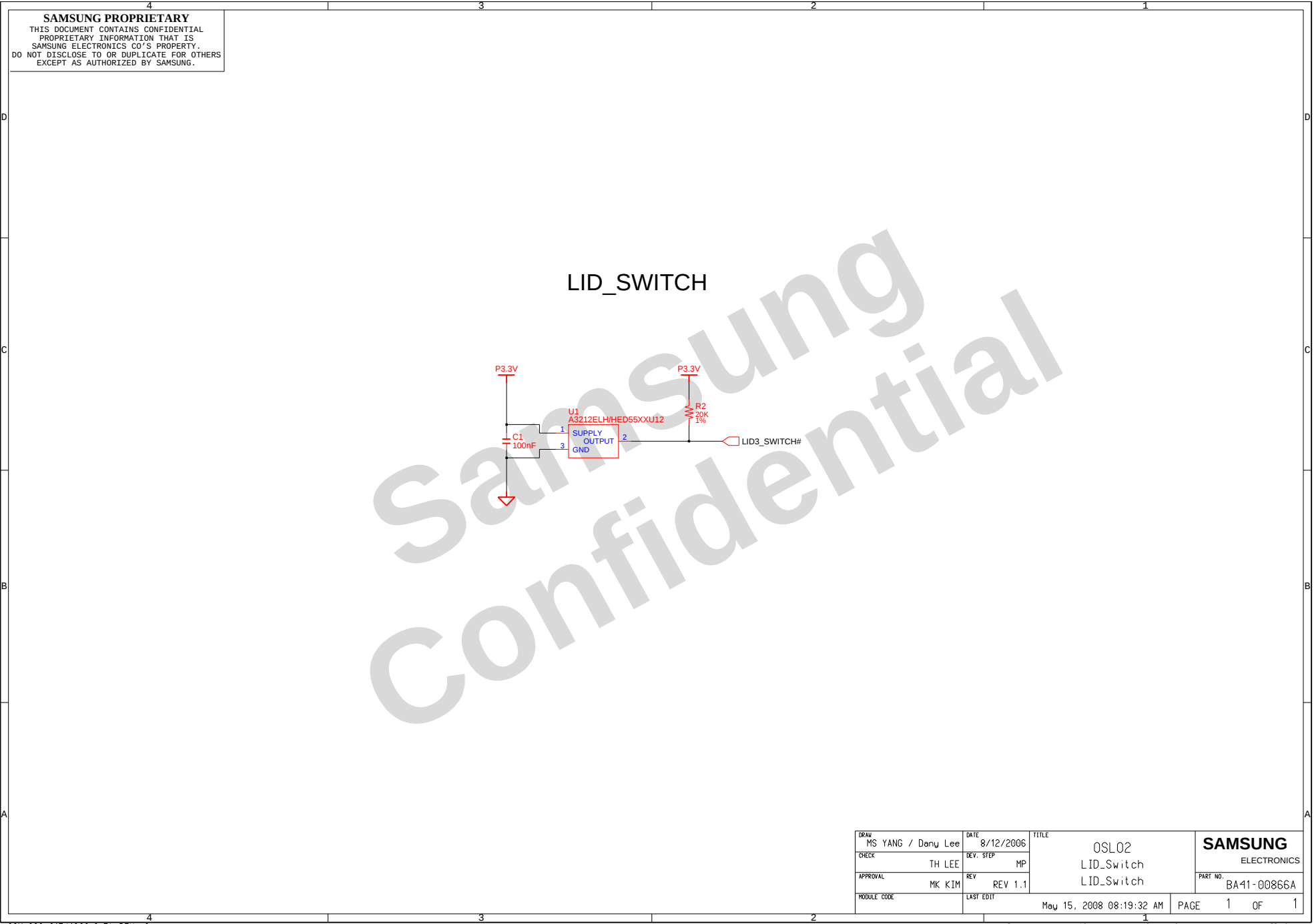
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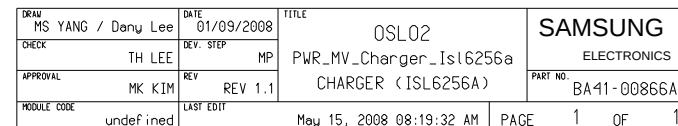
ADAPTERIN/CHARGING LED



DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02 LED_Switch LED_Switch	SAMSUNG ELECTRONICS PART NO. BA41-00866A
CHECK TH LEE	DEV. STEP MP		
APPROVAL MK KIM	REV REV 1.1		
MODULE CODE	LAST EDIT		
May 15, 2008 08:19:32 AM			PAGE 1 OF 1

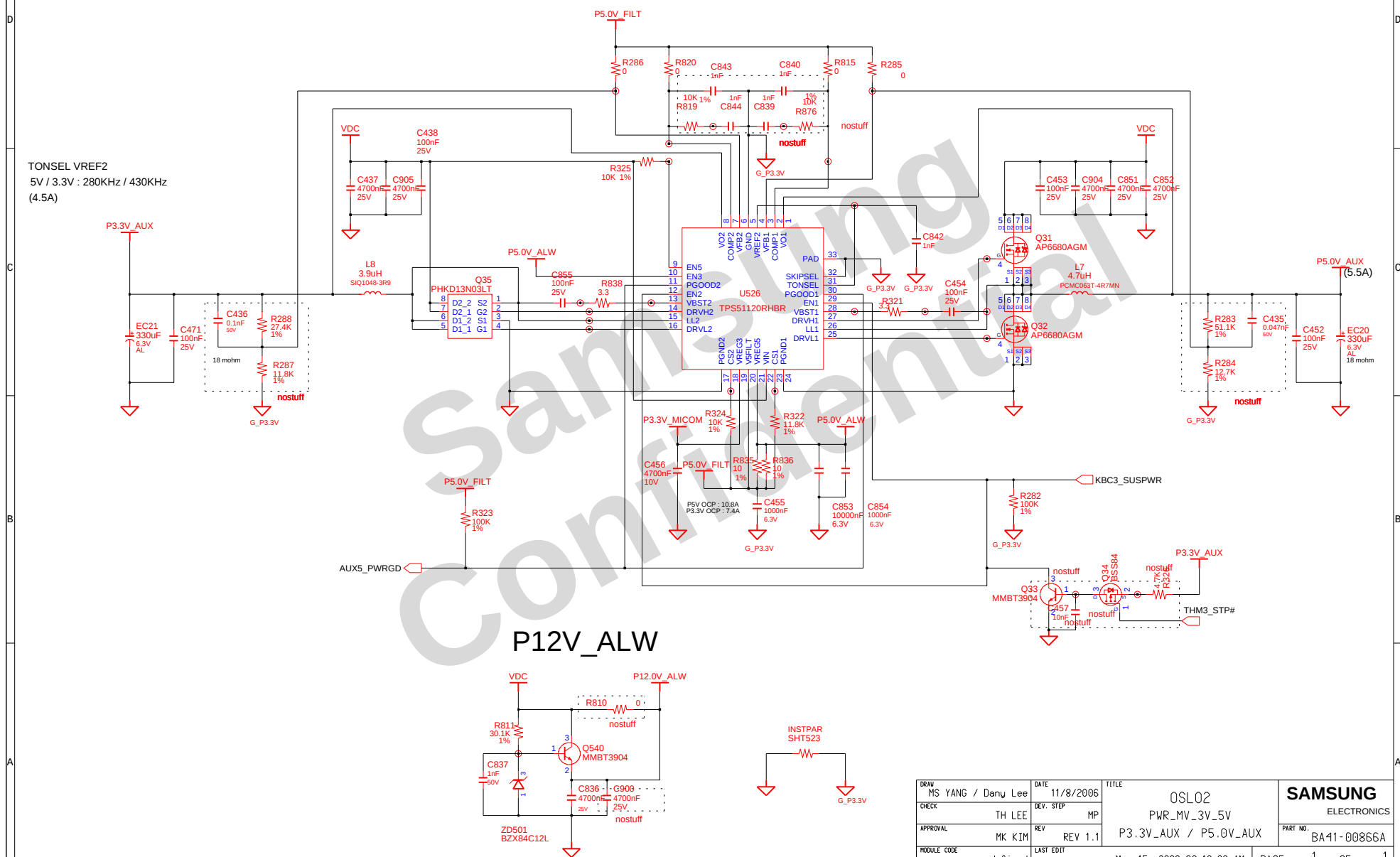


CHARGER & POWER MANAGEMENT

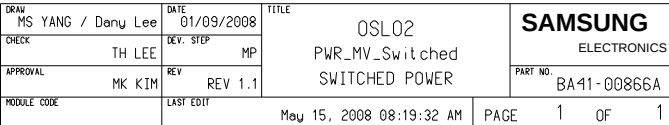


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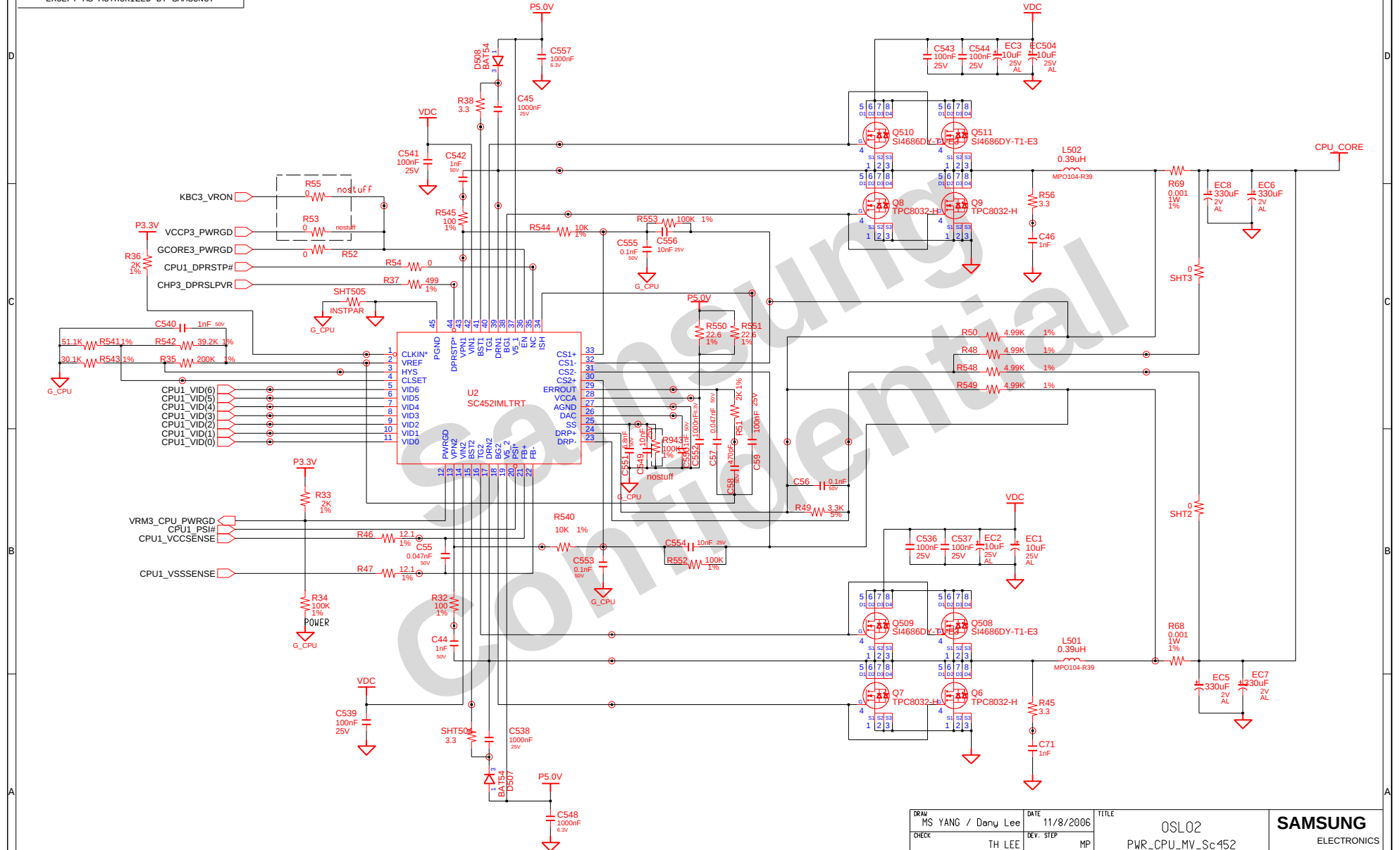
P3.3V_AUX & P5.0V_AUX



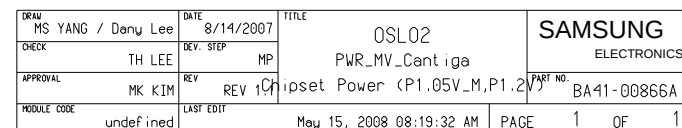
DRAW MS YANG / Dany Lee		DATE 11/8/2006	TITLE OSL02 PWR_MV_3V_5V P3.3V_AUX / P5.0V_AUX		DRAW SAMSUNG	
CHECK TH LEE	DEV. STEP MP	ELECTRONICS				
APPROVAL MK KIM	REV REV 1.1				PART NO.	BA41-00866A
MODULE CODE undefined	LAST EDIT May 15, 2008 08:19:32 AM				PAGE	1



CPU VRM [SEMTECH]



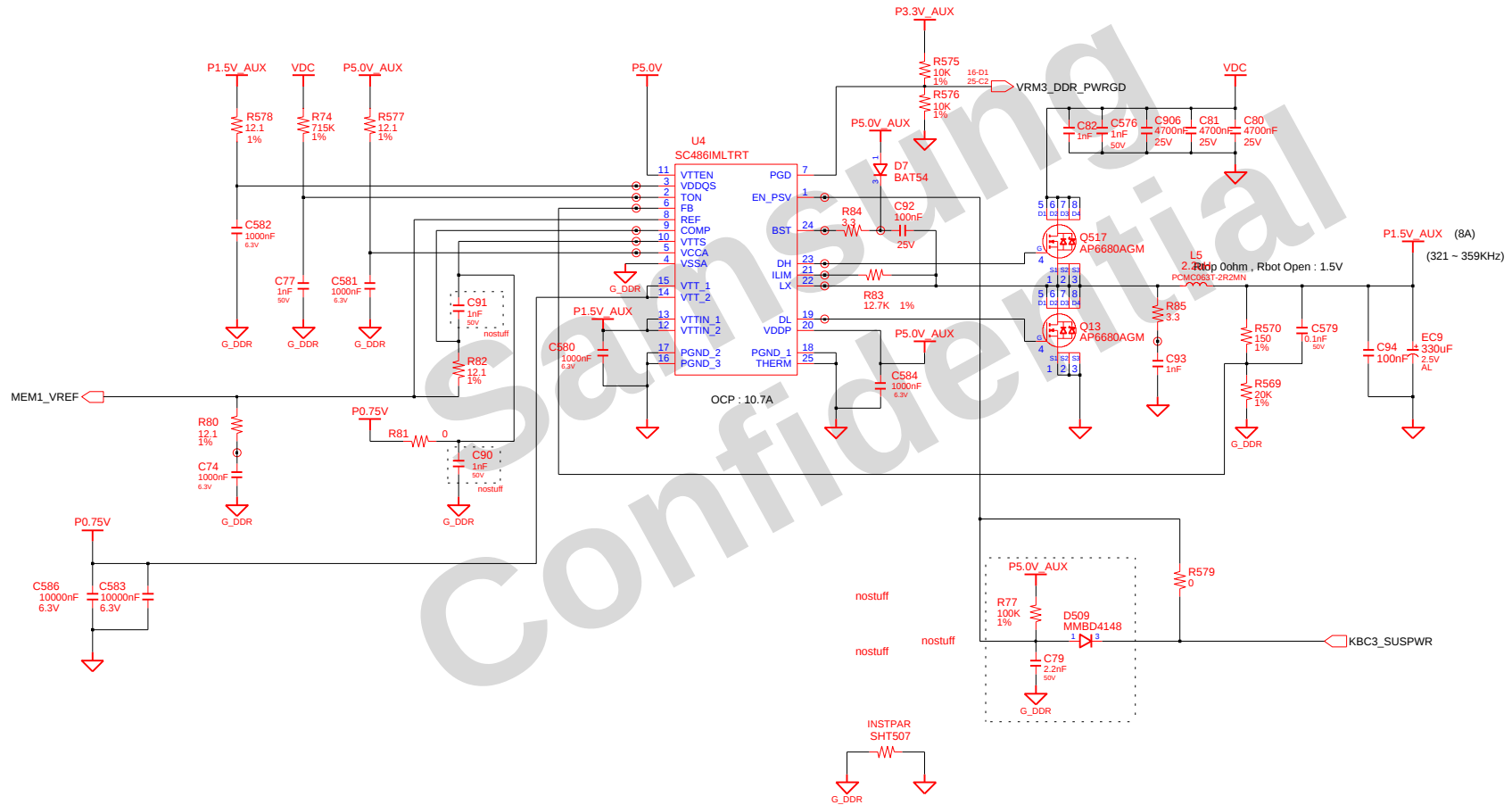
DRAW	MS YANG / Dany Lee	DATE	11/8/2006	TITLE	OSL02	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK	TH LEE	DEV. STEP	MP		PWR_CPU_MV_Sc452	
APPROVAL	MK KIM	REV	1.1		CPU1 VRM (IMVP6+)	
MODULE CODE	undefined	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE	1 OF 1	



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DDR3 Power

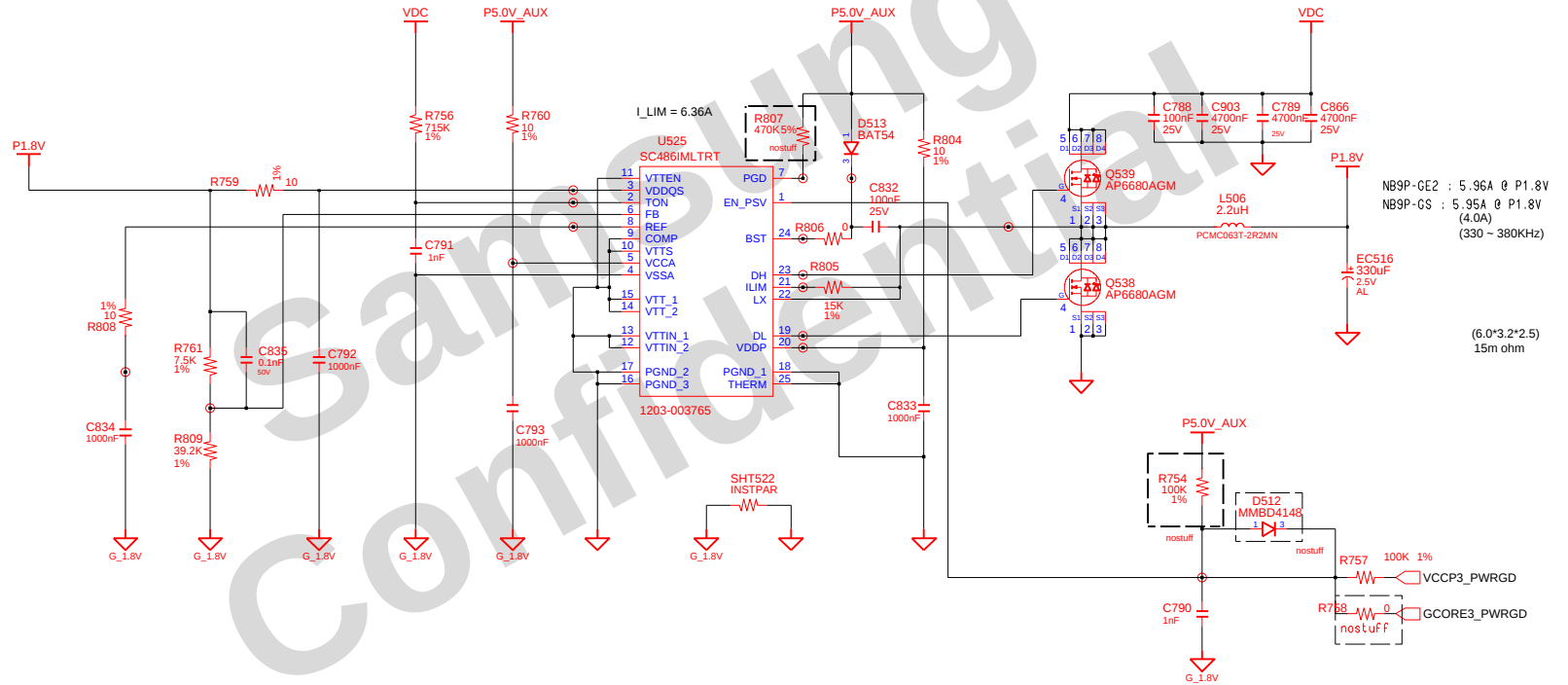


DRAW	MS YANG / Dany Lee	DATE	11/8/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP		PWR_MV_Memory	
APPROVAL	MK KIM	REV	1.1		DDR3 POWER (P1.5V_AUX)	PART NO.
MODULE CODE	undefined	LAST EDIT				BA11-00866A
				May 15, 2008 08:19:32 AM	PAGE	1 OF 1

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P1.8V (External Gfx Memory)

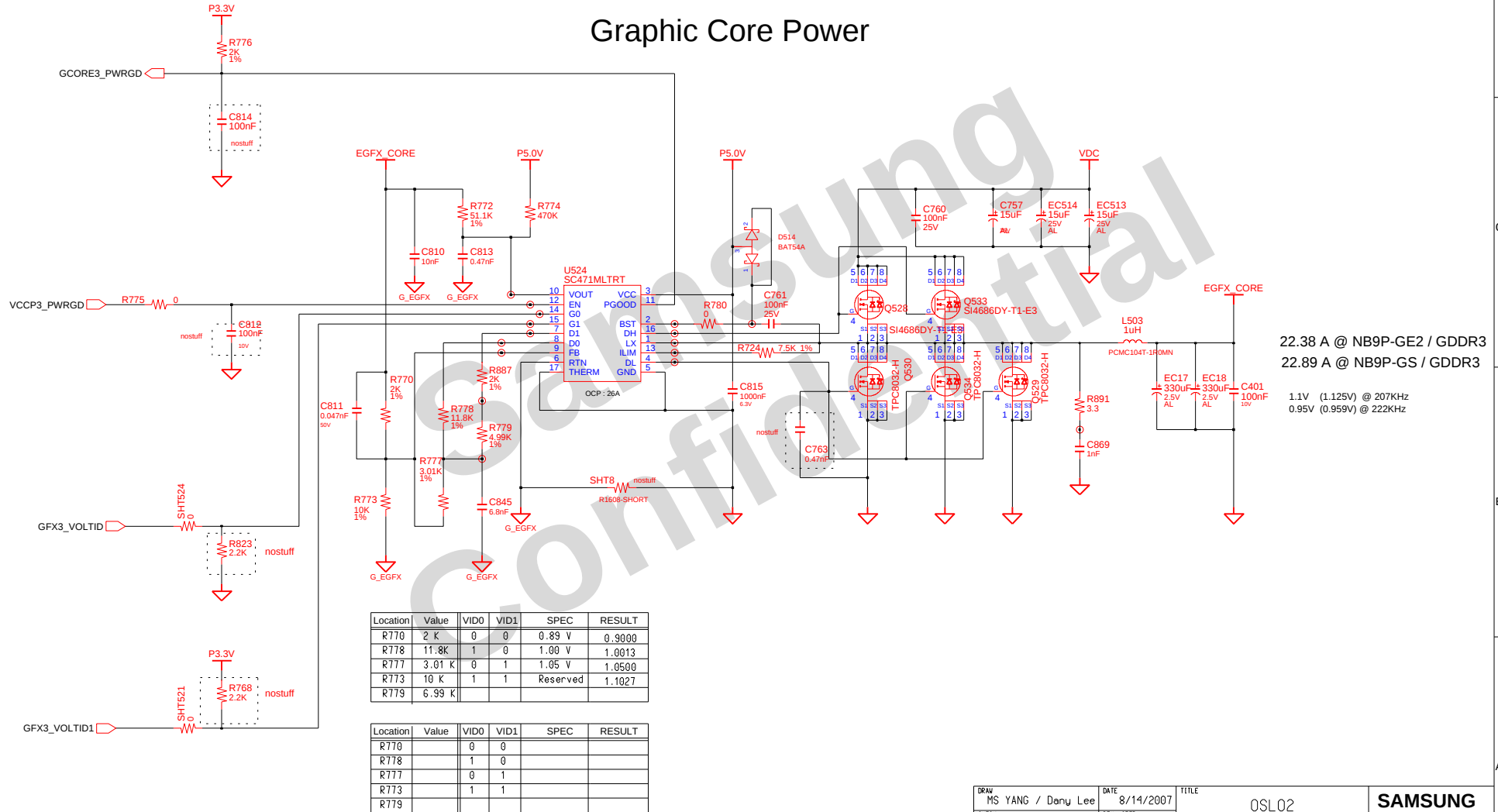


DRW MS YANG / Dany Lee	DATE 8/14/2007	TITLE OSL02 PWR_Gfx_MV_Ext Ext Gfx Memory(SC486)	SAMSUNG ELECTRONICS
CHECK TH LEE	DEV. STEP MP		PART NO. BA11-00866A
APPROVAL MK KIM	REV REV 1.1		
MODULE CODE	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE 1 OF 2

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Graphic Core Power



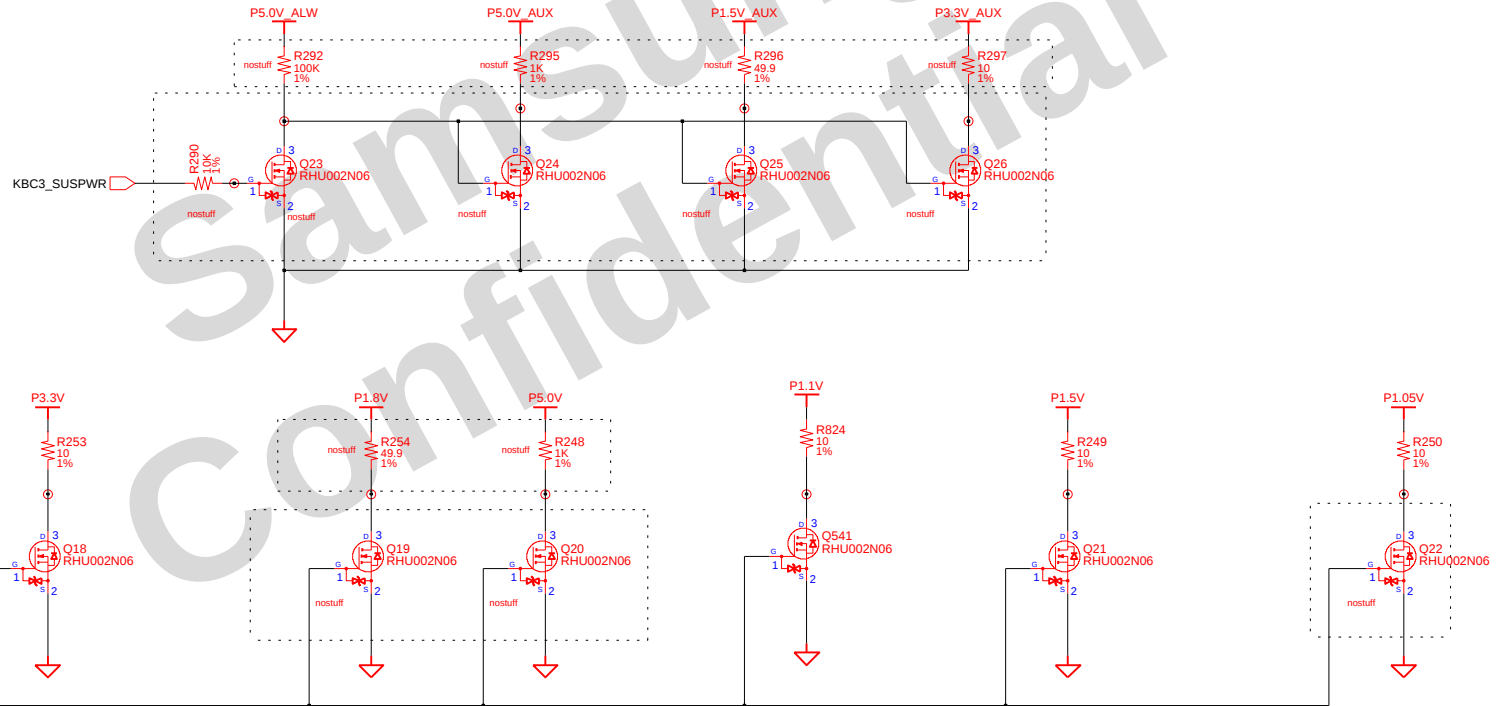
DRW MS YANG / Dany Lee	DATE 8/14/2007	TITLE OSL02 PWR_Gfx_MV_Ext Ext Gfx Core(SC471)	SAMSUNG ELECTRONICS PART NO. BA41-00866A
CHECK TH LEE	DEV. STEP MP		
APPROVAL MK KIM	REV REV 1.1		
MODULE CODE	LAST EDIT		

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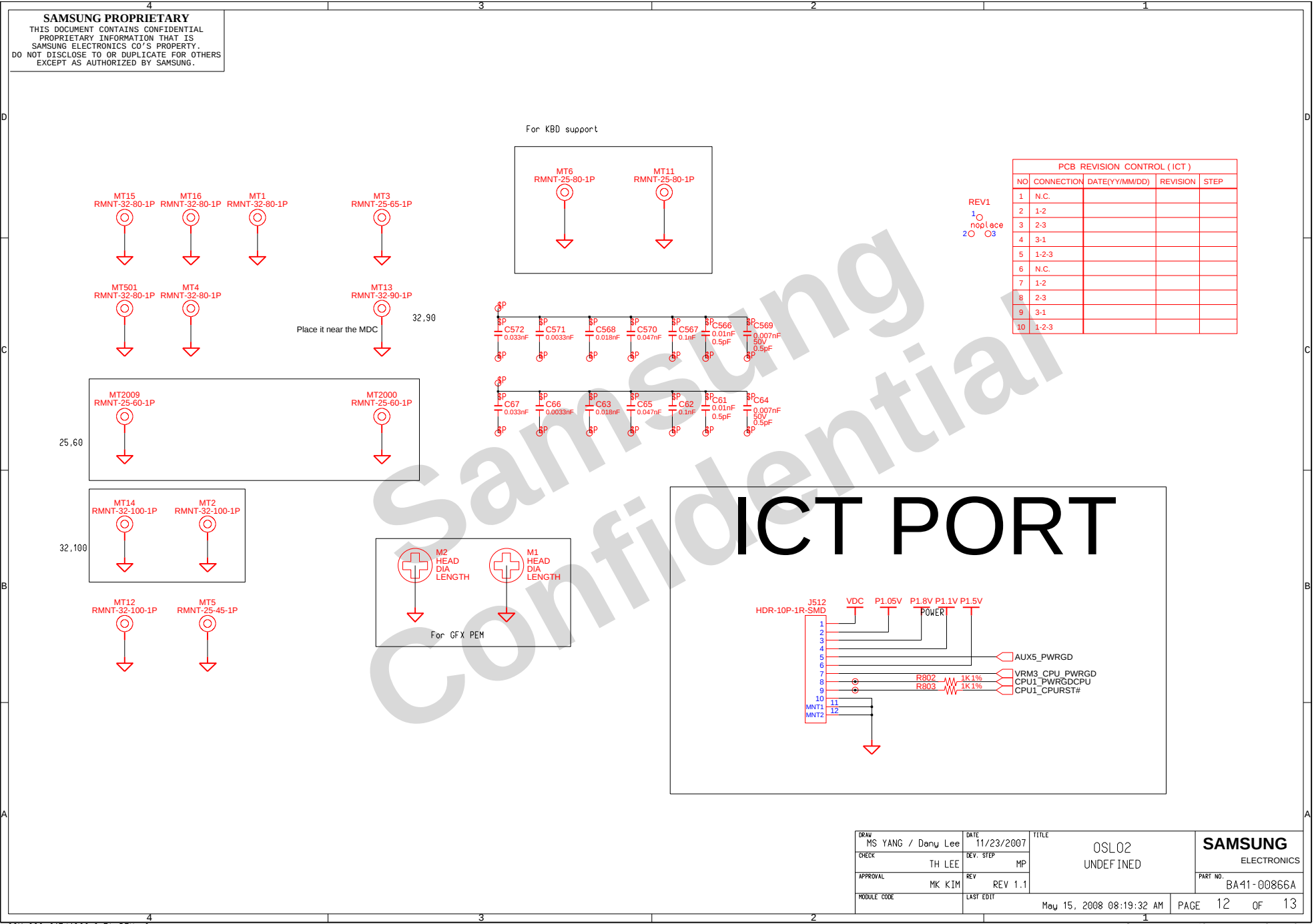
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POWER DISCHARGER



DRAW MS YANG / Dany Lee	DATE 8/14/2007	TITLE OSL02	SAMSUNG ELECTRONICS PART NO. BA41-00866A
CHECK TH LEE	DEV. STEP MP	PWR_MV_DisCharger	
APPROVAL MK KIM	REV REV 1.1	DISCHARGING LOGIC	
MODULE CODE undefined	LAST EDIT	May 15, 2008 08:19:32 AM	
			PAGE 1 OF 1



PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

REV1
1 O nopl ace
2 O O3

[illegible]

```

KBK65_K50(8)
KBK65_K50(9)
KBK65_TCLK
KBK65_TCLK#
KBK65_TCLK#_D
KBK65_TCLK#_D1
CLAN3_L1_LNK100#
CLAN3_L1_LNK100_100#
CLAN3_VPDCLK
CLAN3_VPDDATA

QLDQ3_BKL10N
QLDQ3_BR11
QLDQ3_CQDIO_CLK
QLDQ3_EDIT_DATA
QLDQ3_SWITCH#
QLM03_CLKREQ#
QLP3_LAD(0)
QLP3_LAD(1)
QLP3_LAD(2)
QLP3_LAD(3)
QLP3_LFRAME#

MCMH1_HVREF
MCMH1_HXSUSG
MCMH1_HXSUSG#
MCMH1_DDR_RST#
MCMH3_EXT1510#
MCMH3_EXT1510
MCMH3_TCHSNC#
MCMH3_LCTRL_C
MCMH3_LCTRL_D

SMB3_ALERT#
SMB3_CLK
SMB3_CLK#
SMB3_DATA
SP13_CLK
SP13_CSN
SP13_CS#
SP13_MOSI
SPK5_L+
SPK5_L-
SPK5_L+
SPK5_R+
SPK5_R-
THM3_ALERT#
THM3_STP#
T_R_BUTTON
T_R_BUTTON#

MEM1_VREF
MIN3_CLKREQ#
MI03_BUTTON#

PEP3_BKL1EN
PEP3_HDM1_CLK
PEP3_HDM1_DATA
PEP3_HPD_HDM1
PEP3_LCDVDDIN

PEP3_WAKE#
PL13_RST#
PL13_RST_ORG#

WLN0_LED#

VCCP3_PWRGD
VRN3_DDR_PWRGD

PCP13_CLKRUN#

```

☐ VDC
☐ VDC
☐ VDC
☐ VDC
☐ VDC
☒ VDC_INV
☐ VDC_INV
☐ VCC_CRT
☐ VCC_CRT
☐ P12.0V_ALW
☐ P12.0V_ALW

☐ P5.0V_ALW
☐ P5.0V_ALW
☐ P5.0V_ALW

☐ P5.0V AMP
☐ P5.0V AMP

☐ P5.0V
☐ P5.0V
☐ P5.0V
☐ P5.0V
☐ P5.0V

☐ P5.0V_AUD
☐ P5.0V_AUD

☐ P5.0V_AUX
☐ P5.0V_AUX
☐ P5.0V_AUX
☐ P5.0V_AUX
☐ P5.0V_AUX

☐ P5.0V_FILTER

☐ P475V_AUD
☐ P475V_AUD

☐ P33V_VDD

☐ P33V_EXP
☐ P33V_EXP

☐ P33V_MCD

☐ P33V_MICOM
☐ P33V_MICOM
☐ P33V_MICOM
☐ P33V_MICOM
☐ P33V_MICOM
☐ P33V_MIDA_VDDQ
☐ P33V_MIDA_VDDQ

☐ PRRTC_BAT
☐ PRRTC_BAT

☐ P33V
☐ P33V
☐ P33V
☐ P33V
☐ P33V
☐ P33V_AUX_EXP

☐ P33V_DACA

☐ G_33V

☐ LCD_VDD3V
☐ LCD_VDD3V

☐ G_1.8V

☐ P18V
☐ P18V
☐ P18V
☐ P18V
☐ P18V
☐ P18V_FBDVDQ
☐ P18V_FBDVDQ

[illegible]

TP21801  P0.75V
TP21802  VDD_5.0V

TP21803  ADT3_SEL#
TP21804  CHP3_USBPWRON#
TP21798  ITM3_CLKREQ#
TP21799  KBC3_PRECHG
TP21800  KBC3_USBPWRON#

○KBC3_CHG2600
 ○MCD3_SDDATA0
 ○MCD3_SDDATA1
 ○MCD3_SDDATA2
 ○MCD3_SDDATA3
 ○MCD3_XDDATA0
 ○MCD3_XDDATA1
 ○MCD3_XDDATA2
 ○MCD3_XDDATA3
 ○MCD3_XDDATA4
 ○MCD3_XDDATA5
 ○MCD3_XDDATA6
 ○MCD3_XDDATA7
 ○MCD3_MSDATA2_S
 ○MCD3_MSDATA1_X
 ○MCD3_MSDATA3_X
 ○MCD3_SDCLK_MSB
 ○MCD3_XDCLK_MSC
 ○MCD3_MSINS#
 ○MCD3_SDCD#
 ○MCD3_XDALE
 ○MCD3_XDCD#
 ○MCD3_XDCE#

- ☐ 0.7VDDQDQ
- ☐ 0.7VDDQDQ
- ☐ CPU_CORE
- ☐ CPU_CORE
- ☐ AD_DC
- ☐ AD_DC
- ☐ AD_DC
- ☐ AD_DC
- ☐ AD_CHG_REF
- ☐ FB_PLLVDDQ
- ☐ EGFX_CORE
- ☐ EGFX_CORE
- ☐ PEX_PLLVDD
- ☐ G_AUD
- ☐ G_AUD
- ☐ G_AUD
- ☐ G_AUD
- ☐ G_AUD
- ☐ G_CHG
- ☐ G_CHG
- ☐ G_DDR
- ☐ G_DDR
- ☐ G_EGFX
- ☐ G_MIC
- ☐ G_MIC
- ☐ G_P1.1V

GROUND
GROUND
GROUND
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GROUND

○KBC3_CHG2600
 ○MCD3_SDDATA0
 ○MCD3_SDDATA1
 ○MCD3_SDDATA2
 ○MCD3_SDDATA3
 ○MCD3_XDDATA0
 ○MCD3_XDDATA1
 ○MCD3_XDDATA2
 ○MCD3_XDDATA3
 ○MCD3_XDDATA4
 ○MCD3_XDDATA5
 ○MCD3_XDDATA6
 ○MCD3_XDDATA7
 ○MCD3_MSDATA2_S
 ○MCD3_MSDATA1_X
 ○MCD3_MSDATA3_X
 ○MCD3_SDCLK_MSB
 ○MCD3_XDCLK_MSC
 ○MCD3_MSINS#
 ○MCD3_SDCD#
 ○MCD3_XDALE
 ○MCD3_XDCD#
 ○MCD3_XDCE#

any Lee	DATE 11/23/2
TH LEE	DEV. STEP
	PCN

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